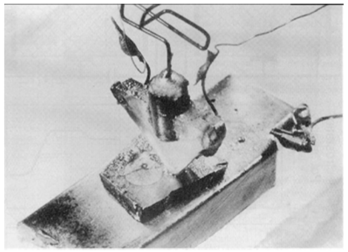
ECE428 :

Programmable ASIC Design

Haibo Wang
ECE Department
Southern Illinois University
Carbondale, IL 62901

The evolution of Integrated Circuits

- 1948: Invention of transistor (Bell Labs)

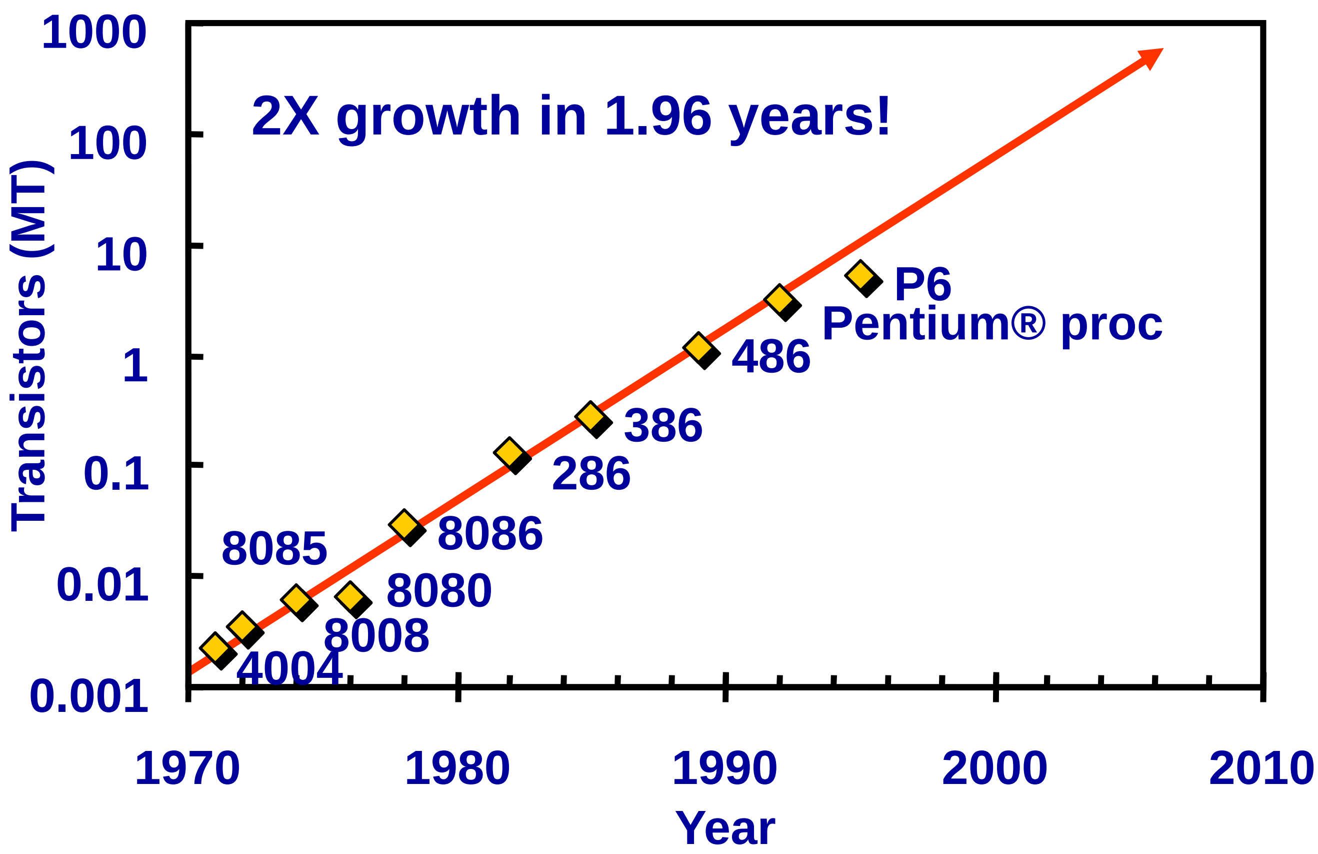


Source Bell Labs

- 1958: Invention of Integrated Circuits
  - — The idea of making a whole circuit-transistors, wires, and everything else-was invented by Jack Kilby at Texas Instruments and Robert Noyce at Fairchild Semiconductor almost at the same time.

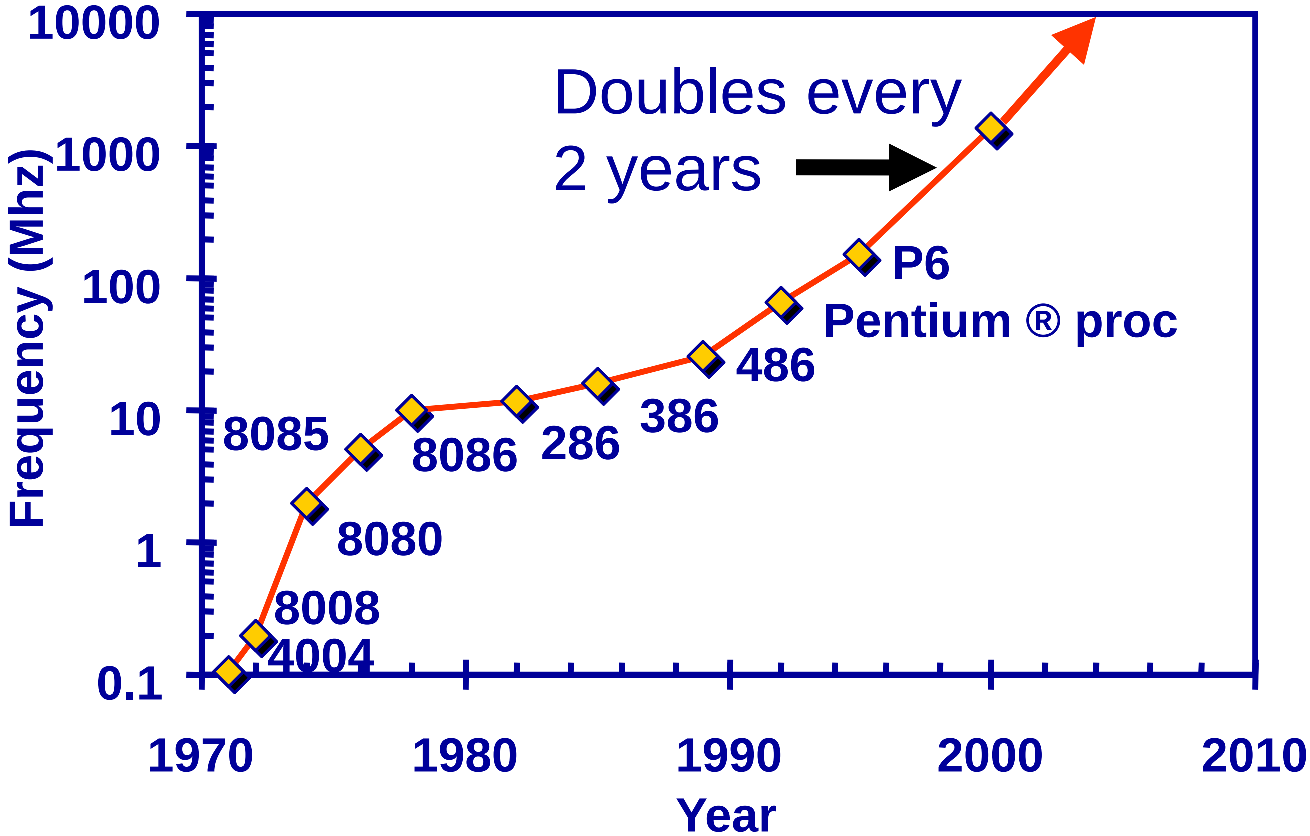
- 1965: Moore's Law
  - — In 1965, Gordon Moore at Intel made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law in Microprocessors



Source from http://infopad.eecs.berkeley.edu/~icdesign

Clock frequencies of Microprocessors



Source from http://infopad.eecs.berkeley.edu/~icdesign

Classifications of Integrated Circuits

- Microprocessors
- Memory chips (SRAM, DRAM, Flash, ROM, PROM)
- Standard Components (74LS..)
- Application-Specific Integrated Circuits
  - Widely used in communication, network, and multimedia systems
  - For a given application, ASIC solutions are normally more effective than the solutions based on running software on microprocessors
  - Many chips in cellular phones, network routers, and game consoles are ASICs
  - Most SoC (Systems-on-a-Chip) chips are ASICs

ASIC Design Methodologies

ASIC Design Methodology

Full-custom design

- This approach is extremely slow, expensive
- It is only used to design very high performance systems

Standard-cell based design

- This approach is reasonable fast, less expensive
- Most ASICs are currently designed using this method

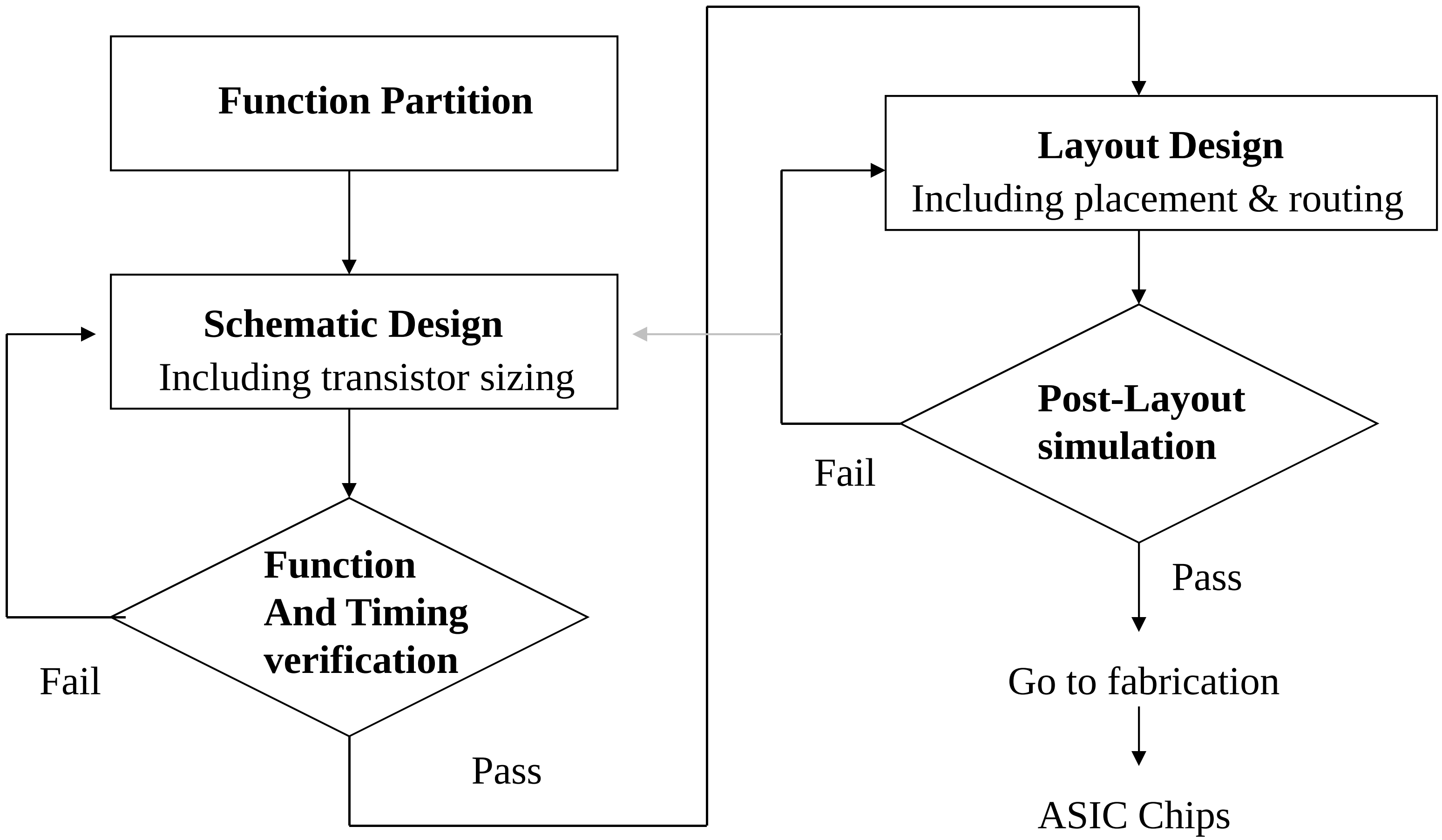
Gate-array based design

- This approach is fast and less expensive
- ASIC performance are relatively slow

FPGA based design

- The design process is very fast and cost effective
- ASIC performance are slow

Full-Custom Design Methodology

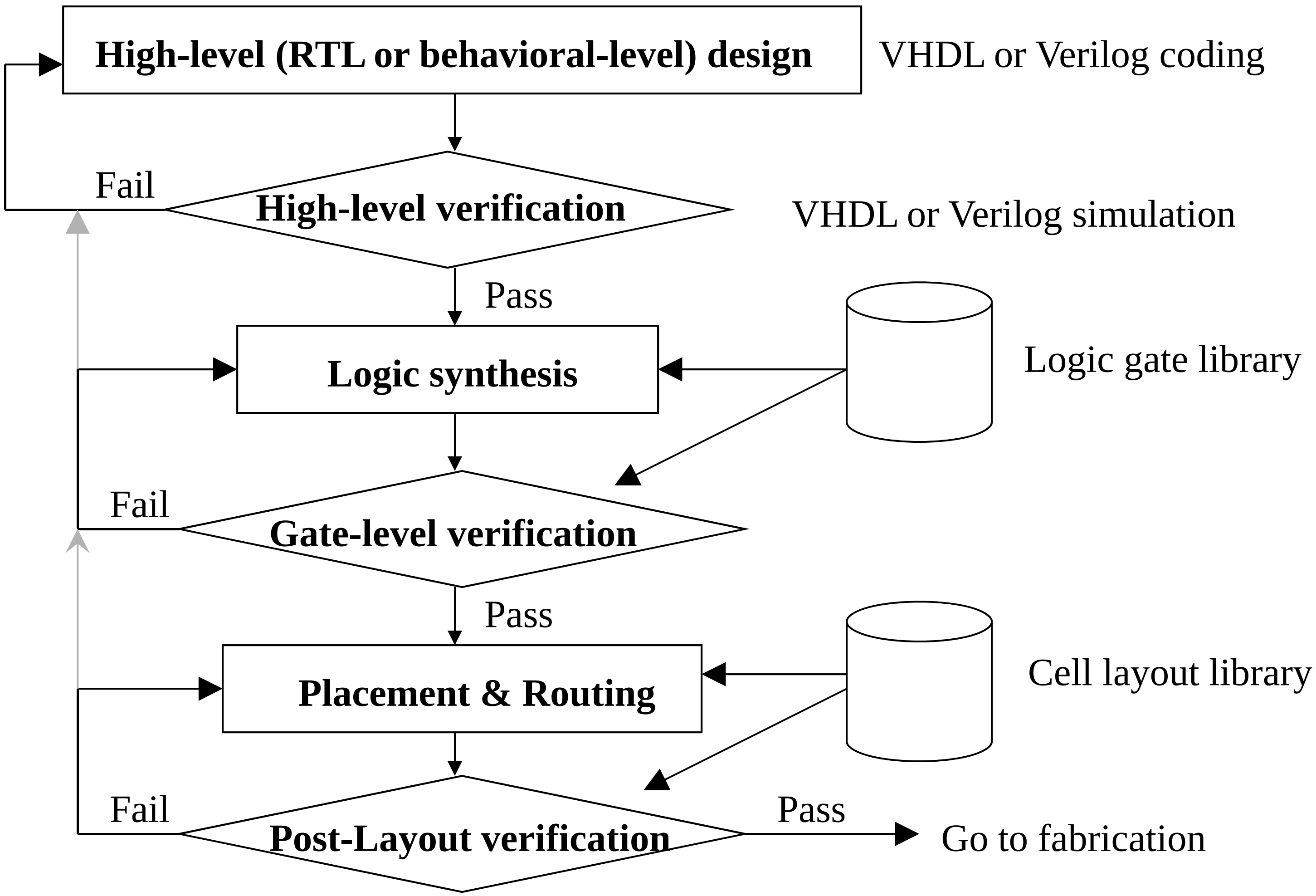


- **It is a time consuming manual process, not pre-developed libraries needed**.

Full-Custom Design Methodology

- Design a chip from scratch.
- Engineers design some or all of the logic cells, circuits, and the chip layout specifically for a full-custom IC.
- Custom mask layers are created in order to fabricate a full-custom IC.
- Advantages: complete flexibility, high degree of optimization in performance and area.
- Disadvantages: large amount of design effort, expensive.

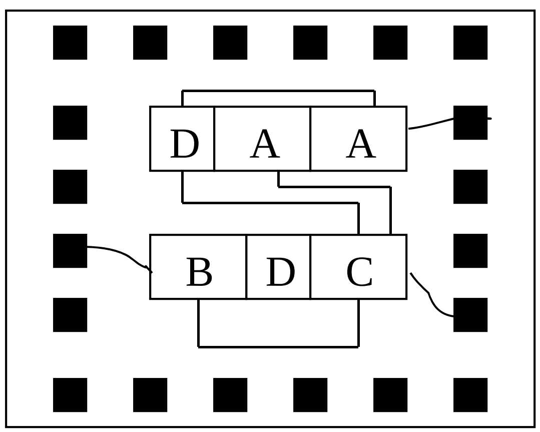
Standard-Cell Based Design Methodology



- **It is highly automated, but need pre-developed libraries**.

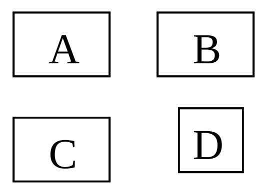
Standard-Cell Based Design Methodology

- Use pre-developed logic cells from standard-cell library as building blocks.
- As full-custom design, all mask layers need to be customized to fabricate a new chip.
- Advantages: save design time and money, reduce risk compared to full-custom design.
- Disadvantages: still incurs high non-recurring-engineering (NRE) cost and long manufacture time.

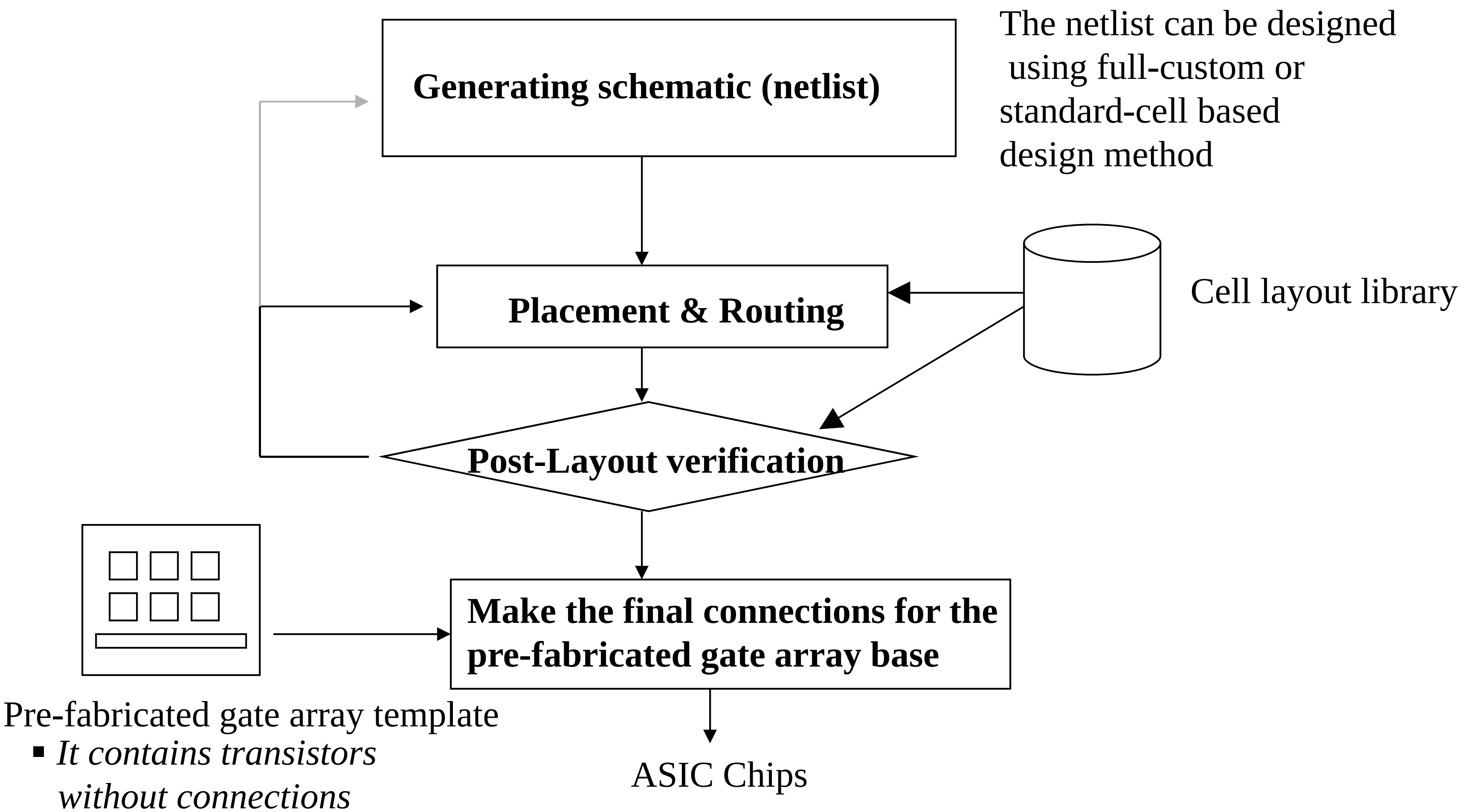


Chip layout

Library Cells



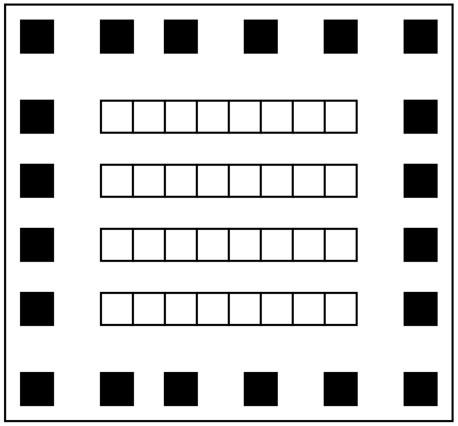
Gate-Array Based Design Methodology



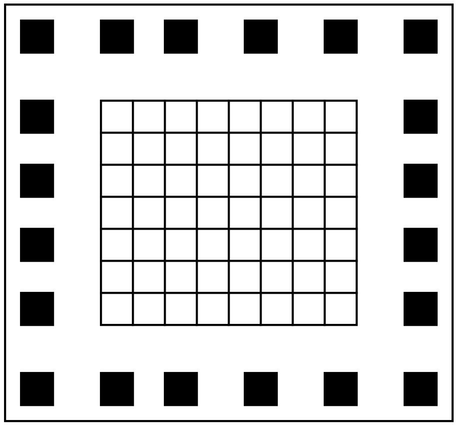
- **This approach is faster than the standard-cell based approach because part of the fabrication process has been complete**.

Gate-Array Based Design Methodology

- Parts of the chip (transistors) are pre-fabricated, and other parts (wires) are custom fabricated for a particular customer's circuit.



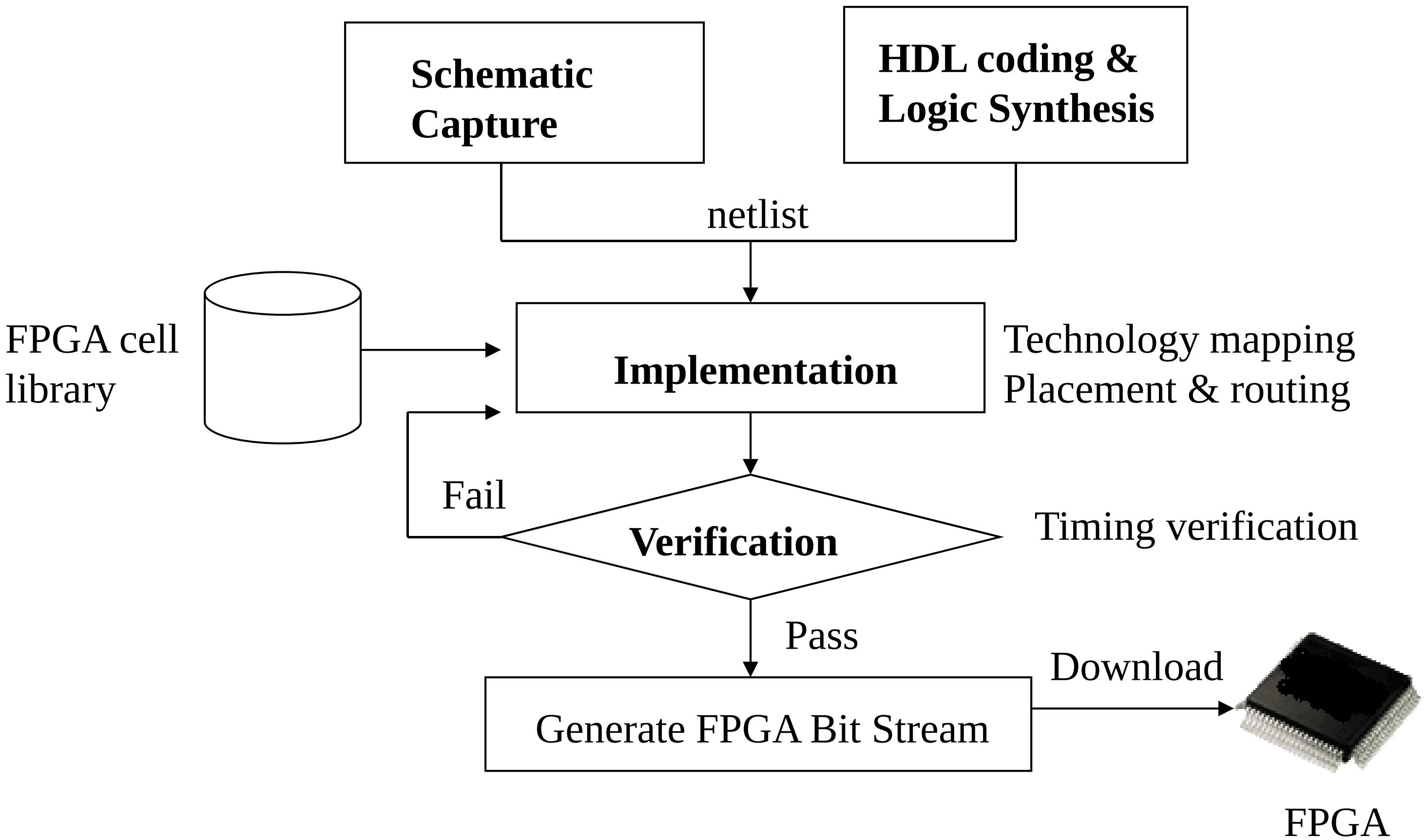
Gate Array



Sea-of-Gates

- Advantages: cost saving (fabrication cost of a large number of identical template wafers is amortized over different customers), shorter manufacture lead time.
- Disadvantages: performance not as good as full-custom or standard-cell-based ICs.

FPGA Based Design Methodology



- **This approach has extremely fast turn-out time since FPGA devices has been fabricated.**

Comparison of Design Methodologies

	Full-custom design	Standard-cell based design	Gate-array based design	FPGA-based design
Speed	+++	++	+	-
Integration density	+++	++	+	--
High-volume device cost	++	++	+	+
low-volume device cost	---	--	+	+++
Custom mask layer	All	All	Some	None
Fabrication time	---	--	-	+++
Time to Market	---	--	++	+++
Risk reduction	---	--	-	+++
Future design modification	---	--	-	+++

+ desirable; - not desirable

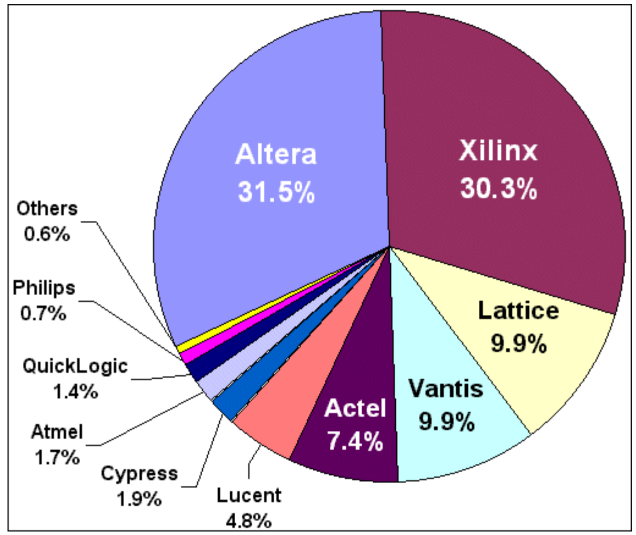
Why do we want FPGAs

- Advantages of using FPGAs
  - Fast turn-out time
  - The ability of re-programming
  - The capability of dynamic reconfiguration

- FPGA Applications
  - Ideal platform for prototyping
  - Providing fast implementation to reduce time-to-market
  - Cost effective solutions for products with small volumes on demand
  - Implementing hardware systems requiring re-programming flexibility
  - Implementing dynamically re-configurable systems

FPGA Market

- Market Share in 1998



  - Total Revenue is above two billion U.S. Dollar

    Source from http://www.optimagic.com/

- Current FPGA revenue is about 3.6B USD.
- Major players include: Xilinx, Altera, Actel, Lattice, Atmel, Cypress, QuickLogic, SiliconBlue

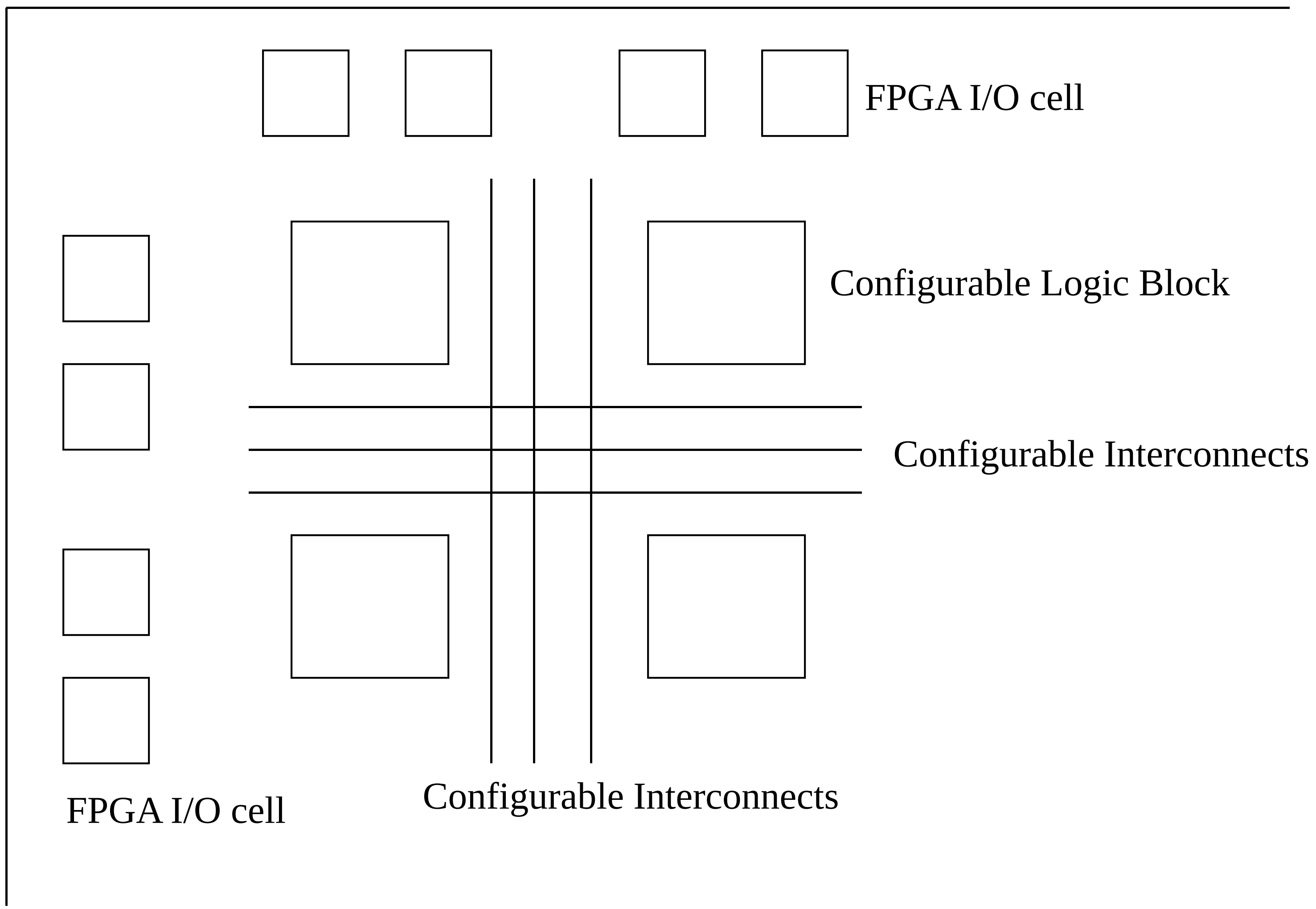
The State-of-Art of FPGAs

- Various types of FPGAs are available for different applications

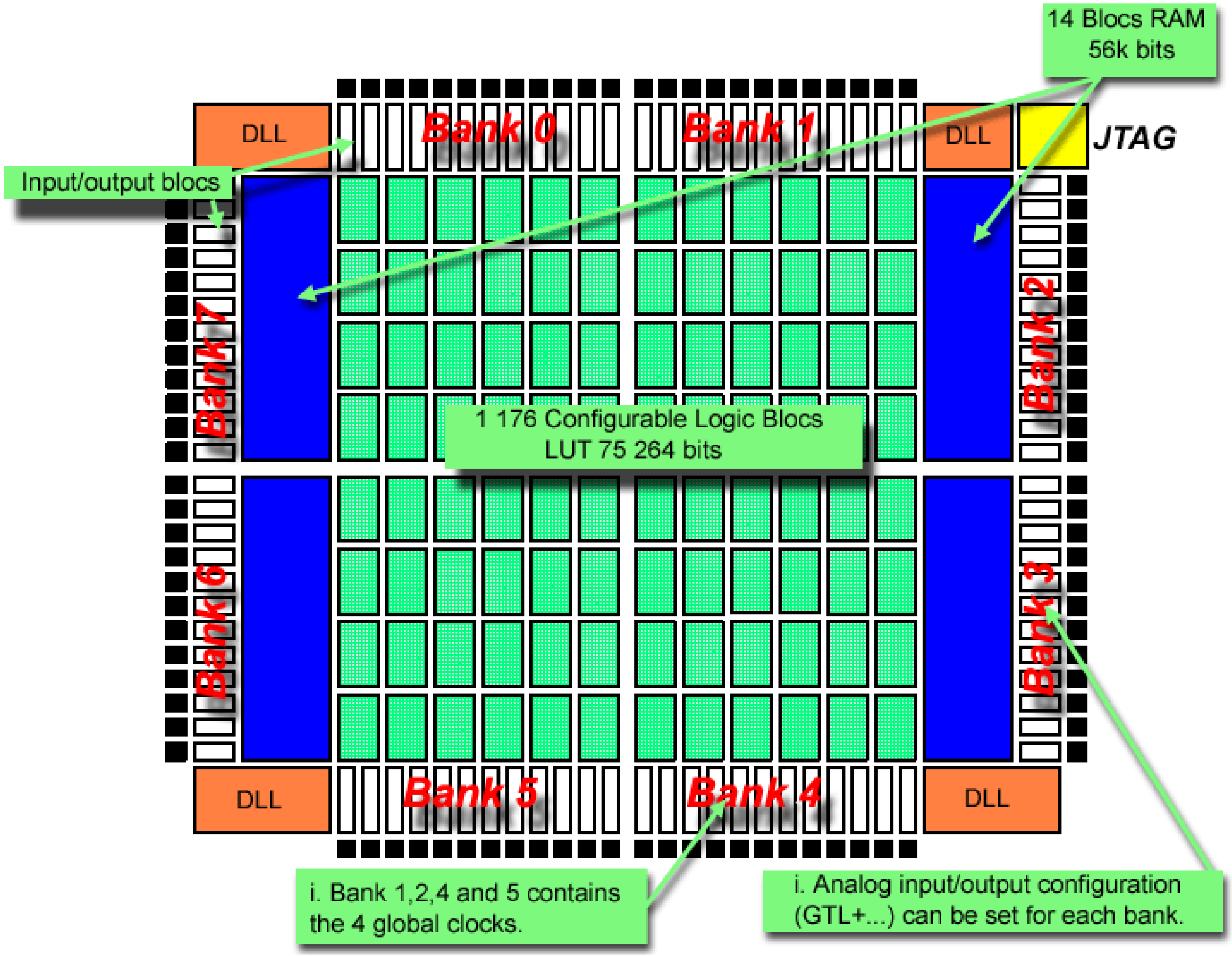
- Modern FPGAs are fabricated using the most advanced technology and are capable to implement very high performance systems
  - For example, the latest Xilinx Virtex-II Pro FPGAs are fabricated using 90 nm technology, containing more than one million gates. Such devices also include PowerPC microprocessor, on-chip memories, and 3.125Gbit/s I/O interfaces.

- Currently, FPGAs are widely used in implementing communication systems, configurable computers, and DSP applications

Typical FPGA Architectures

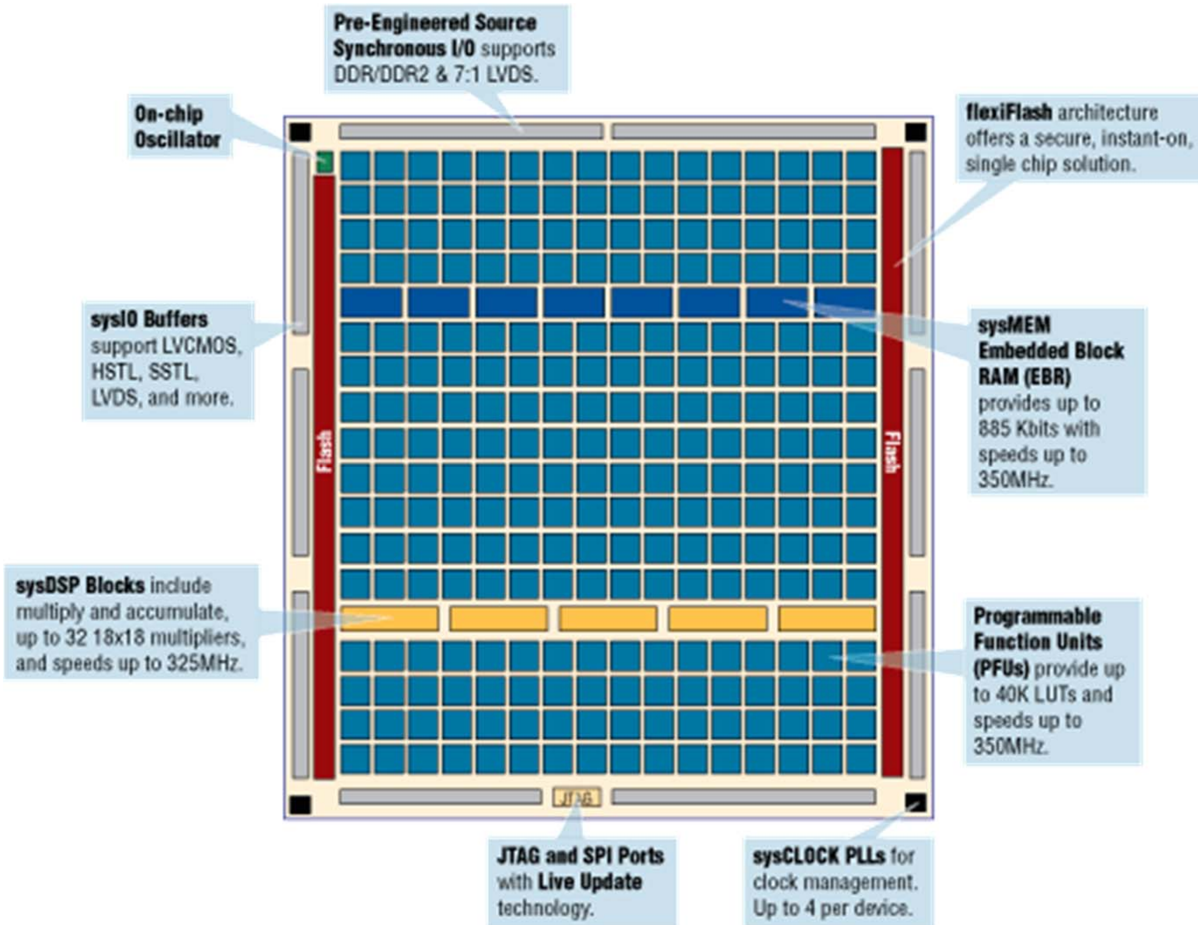


Examples of FPGA Architectures



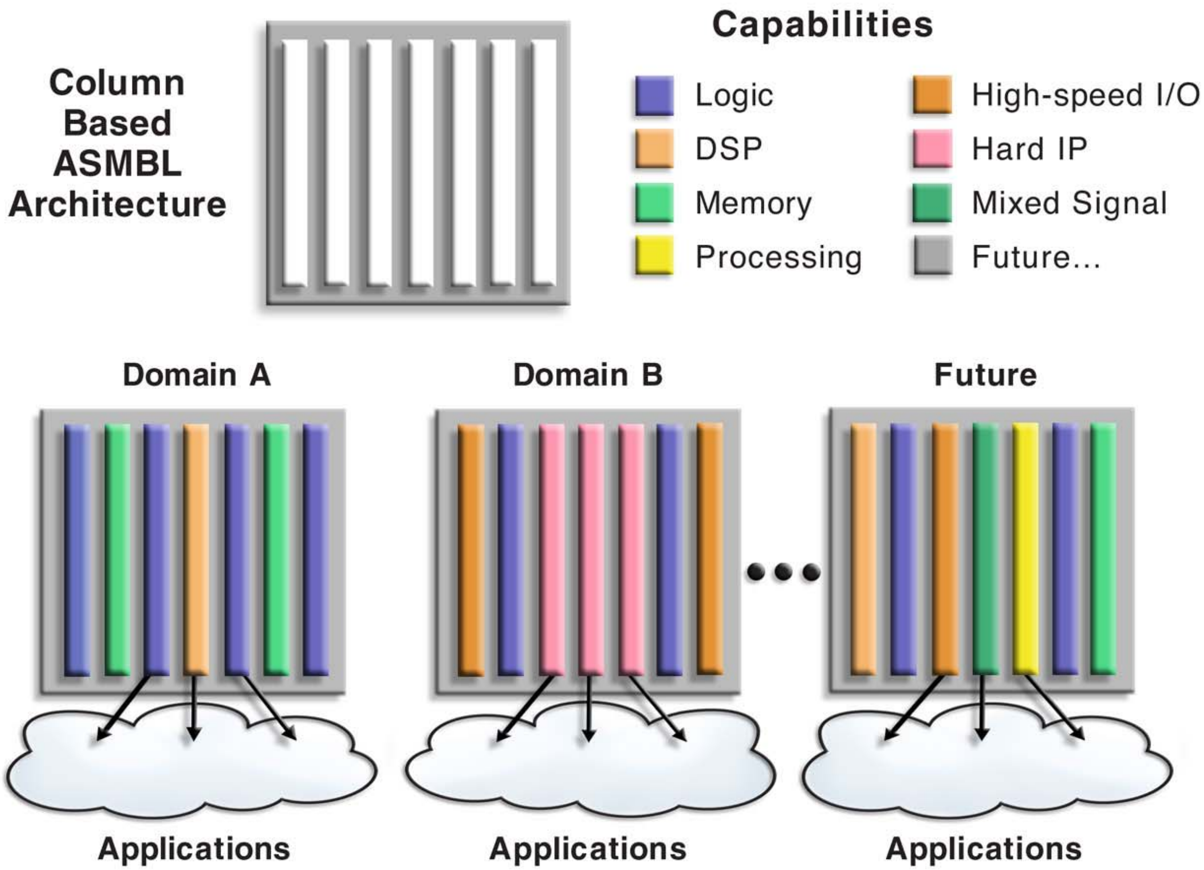
http://www.xilinx.com

Examples of FPGA Architectures



www.latticesemi.com/images/img24483.gif

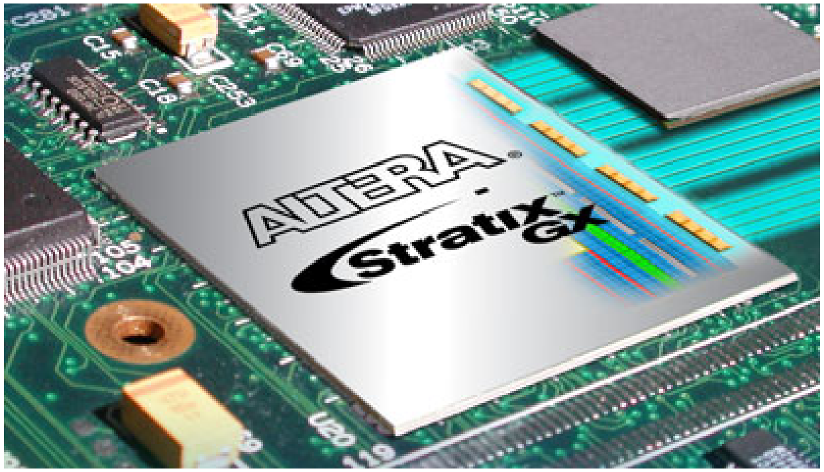
Examples of FPGA Architectures



http://www.xilinx.com

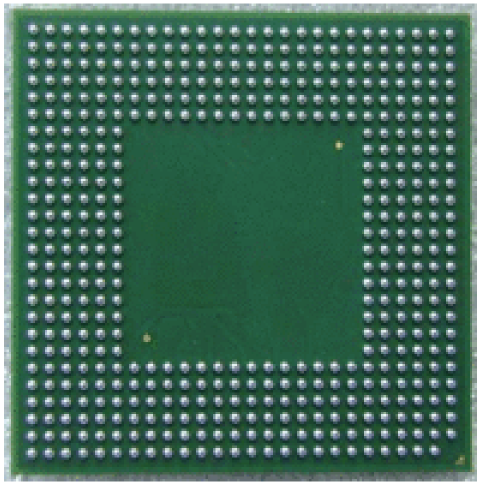
Examples of FPGA Package

- An FPGA with BGA package on PCB



www.altera.com

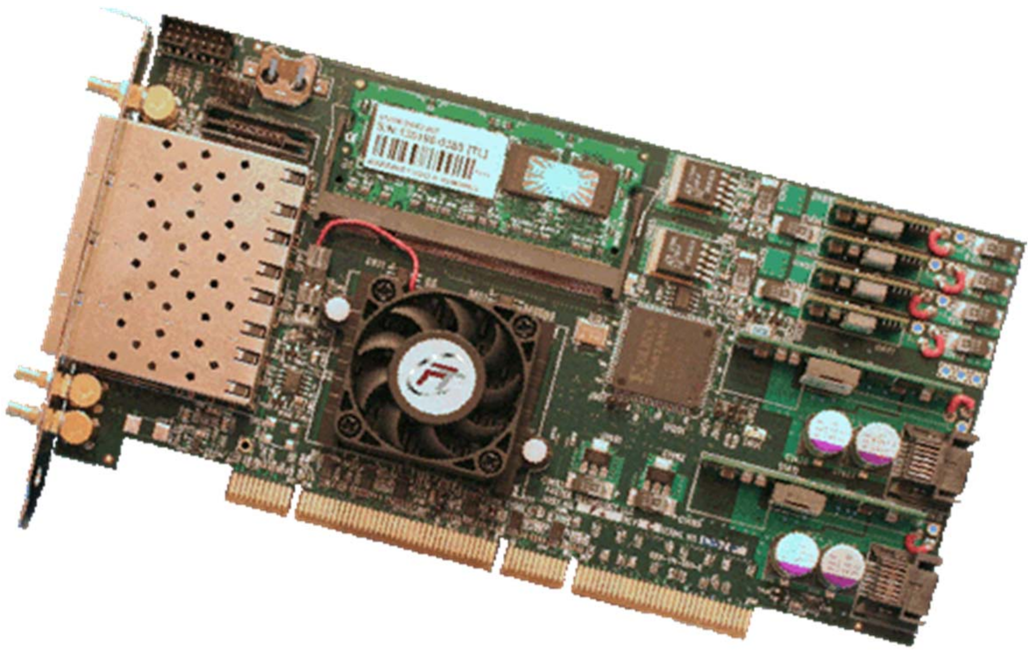
- Back view of Ball Grid Array (BGA)



http://www.bluemelon.org/index.php/Projects/FPGA_design

Examples of FPGA Applications

- Reconfigurable computing & hardware accelerator



http://www.fastertechnology.com/

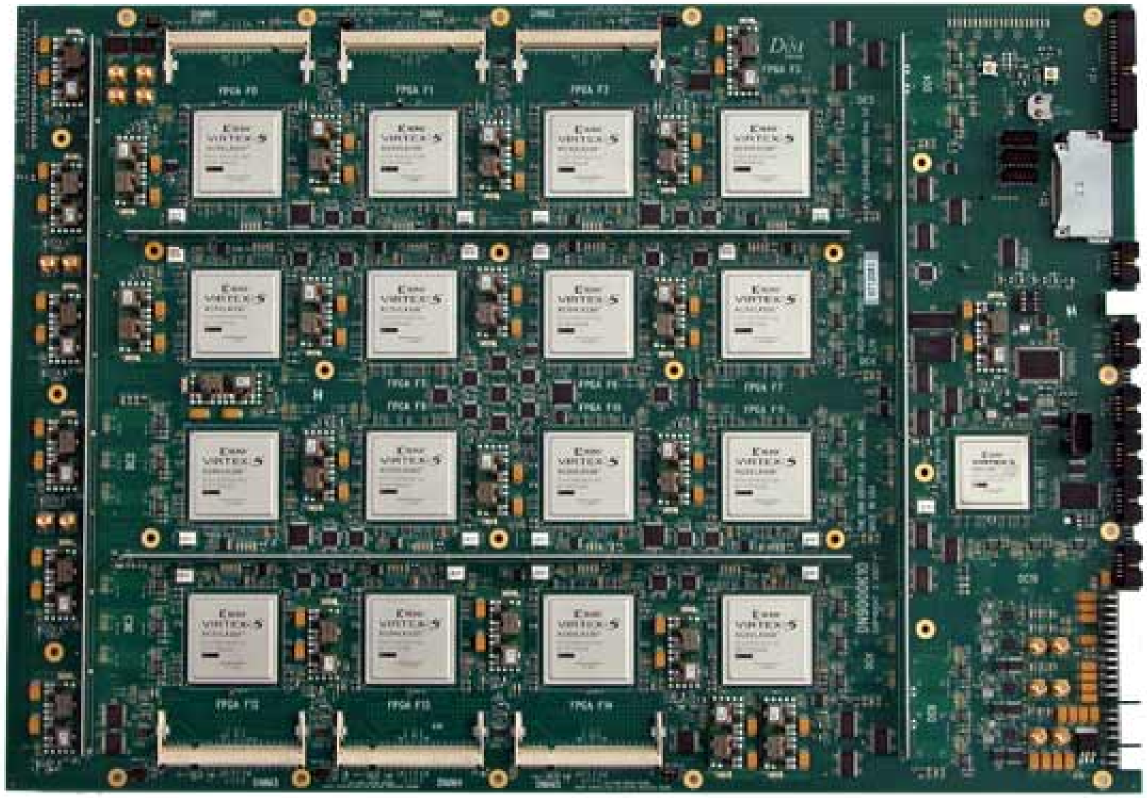
Examples of FPGA Applications

- 40Gbps datapath for internet connection

http://www.xilinx.com/publications/prod_mktg/pn2094.pdf

Examples of FPGA Applications

- Logic emulation



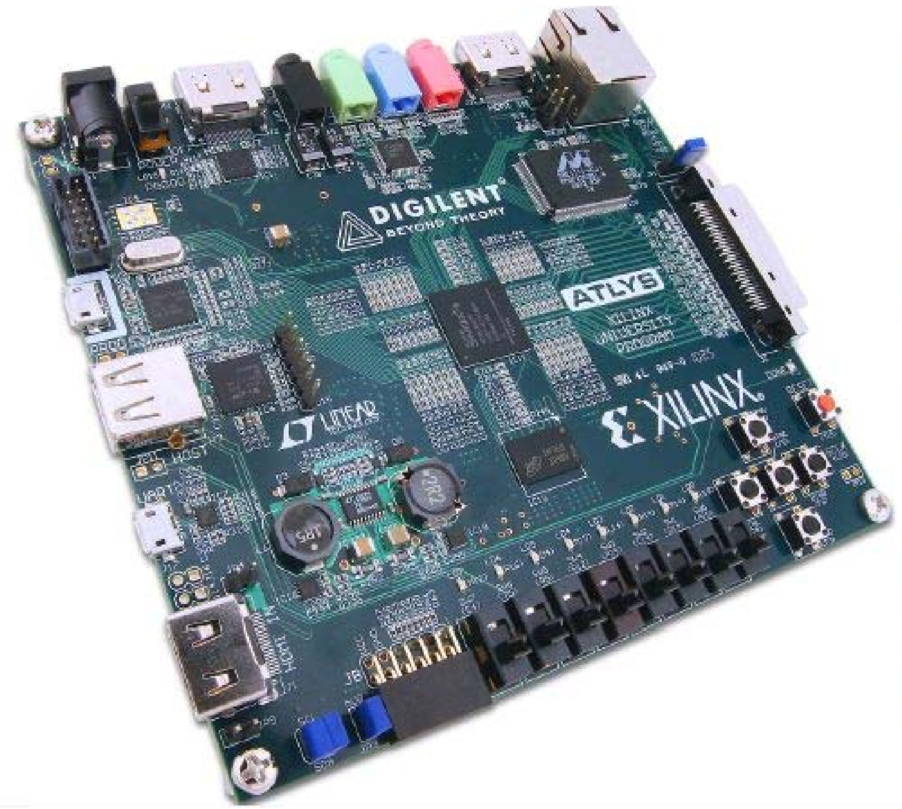
www.applistar.com/top/DN9000K10.jpg

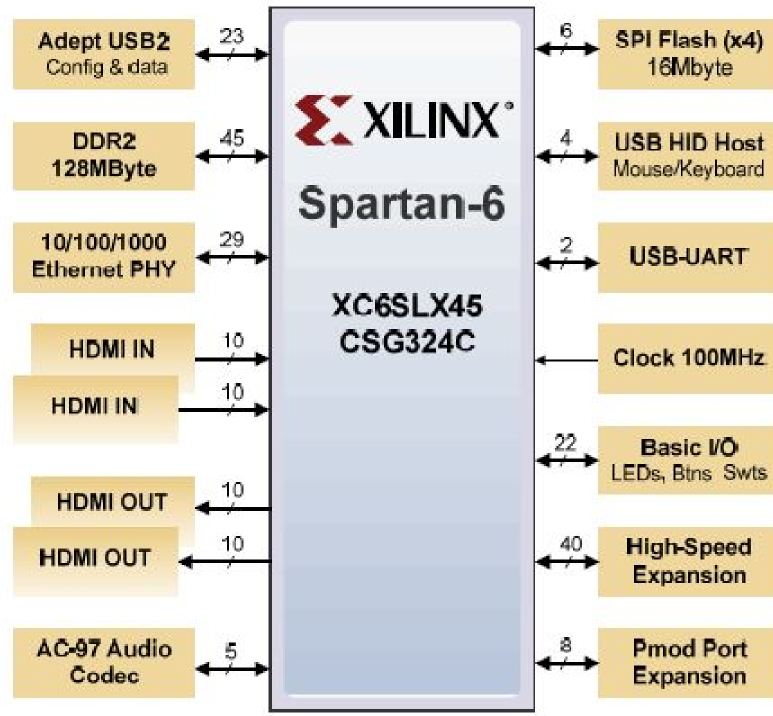
Focus of this course

- **FPGA fundamentals**
  - Basic FPGA components: Configurable logic blocks (CLB), Interconnects, I/O blocks
  - Programming techniques
  - Implementing logic function with look-up table or multiplexers.
- **Essential techniques in modern synchronous ASIC design**
  - Time violations
  - Asynchronous signals in synchronous circuits
  - Coping with multi-clock domains
- **FPGA design for specific applications**
  - FPGA arithmetic circuits
  - FPGA DSP applications
  - FPGA in digital communication applications
  - FPGA microprocessor
- **Four case-studies will be discussed**
  - SDRAM controller, half-tone pixel converter, a biquad low-pass filter and a SPI-USB interface

Hardware used in the course

- Spartan-6 based Atlys board





Exams, Projects, labs & homework

- Two midterm exams and one final
  - Midterm 1 15%, Midterm 2 20% & Final 30%
- Project: SPI and USB interface circuits
  - 15%
- Four labs
  - 10%
- Homework
  - 10%