Issues in ASIC Design with Multi-Clock Domains

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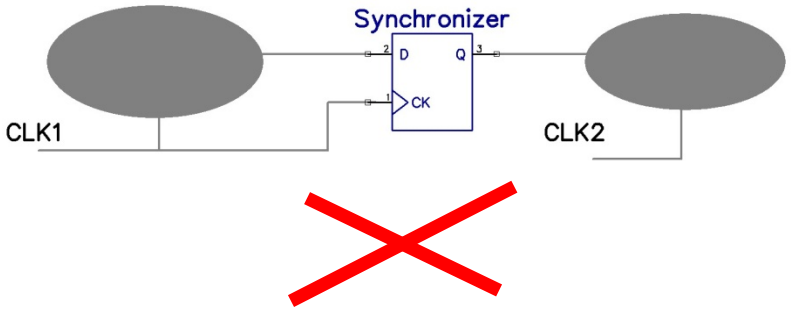
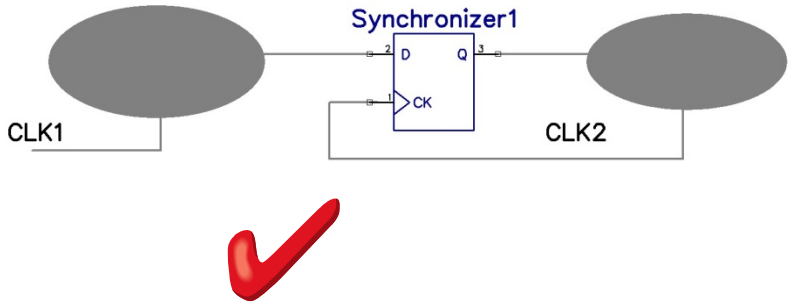
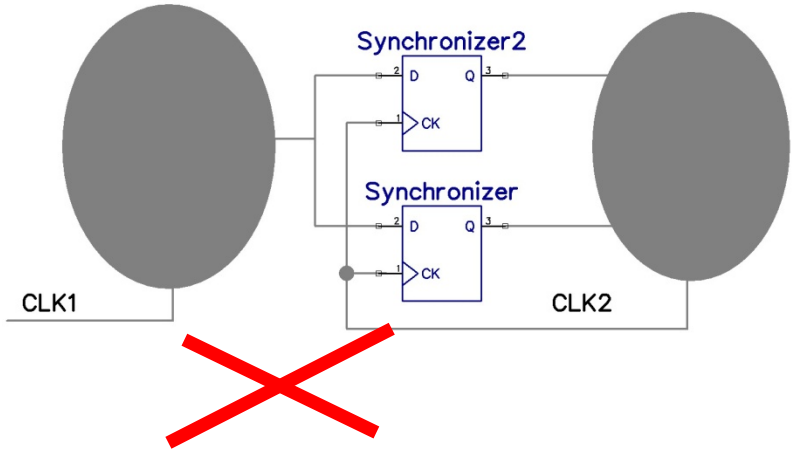
Mistakes in the Use of Synchronizer

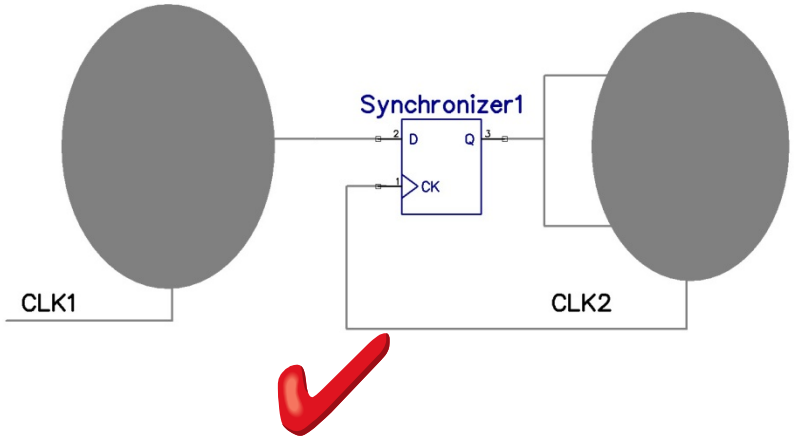
- Does not use the correct clock





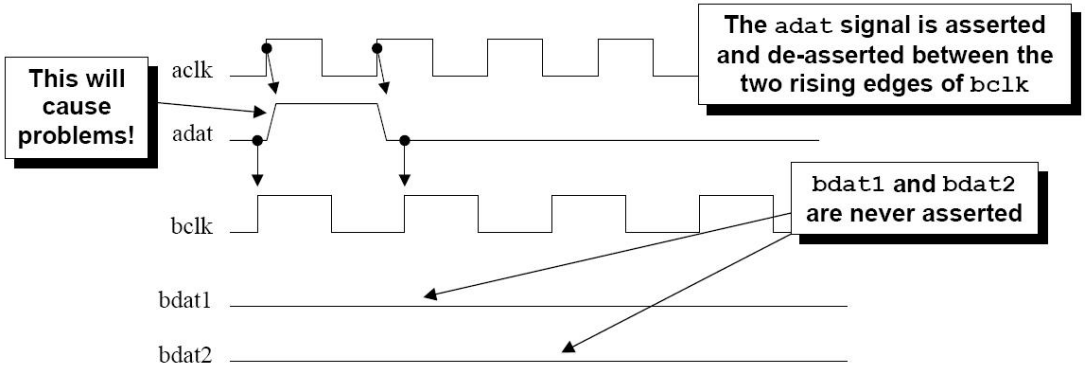
- Synchronize the same signal more than once



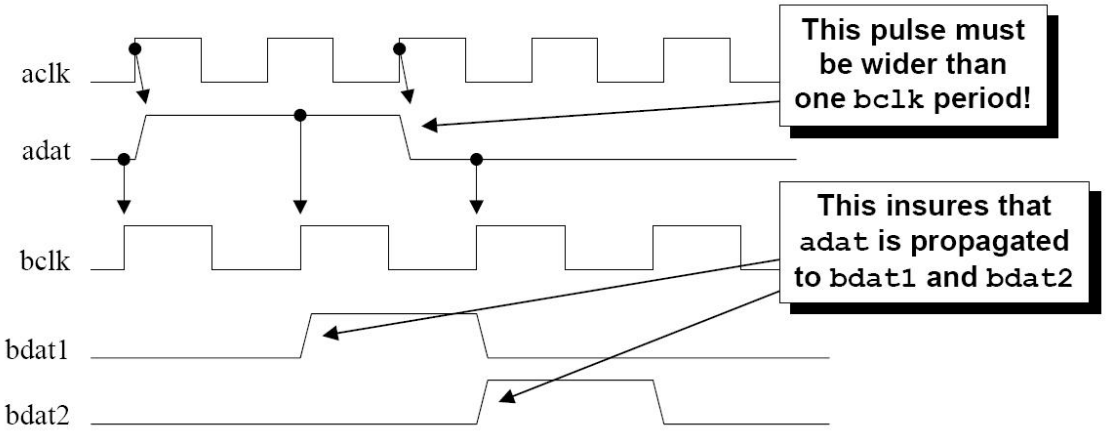


Passing a control signal from slow clock domain to fast clock domain

- The control signal may not be captured by the slow clock domain



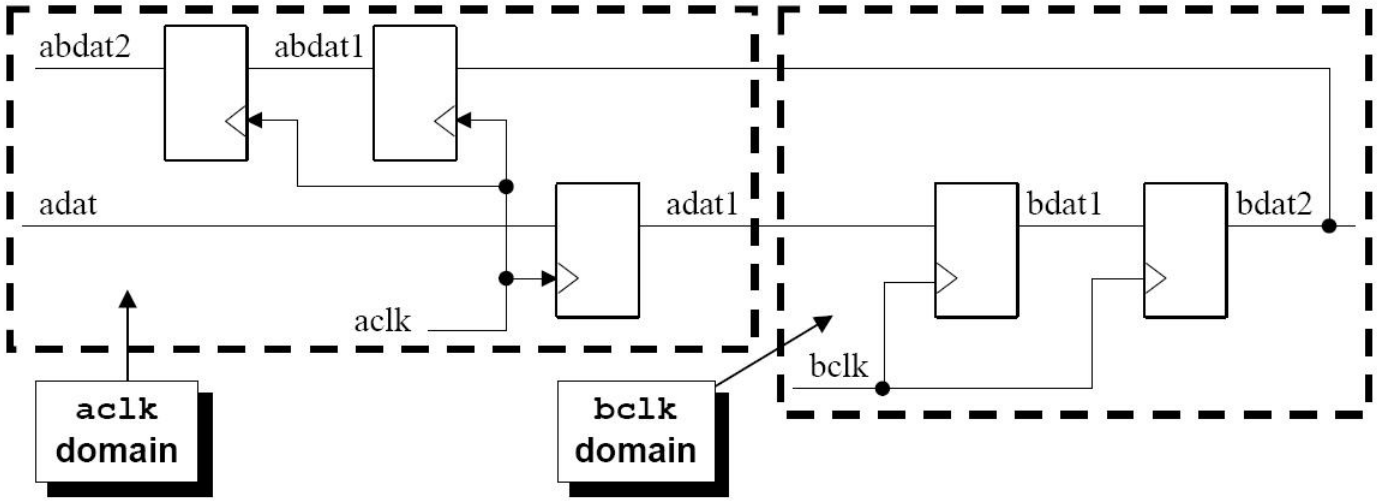
- Assert the control signal for a time period longer than the slow clock period



Source: Clifford Cummings, "Synthesis and Scripting Techniques for Designing Multi Asynchronous Clock Designs"

Passing a control signal from slow clock domain to fast clock domain

- Feedback the control signal as the acknowledge signal

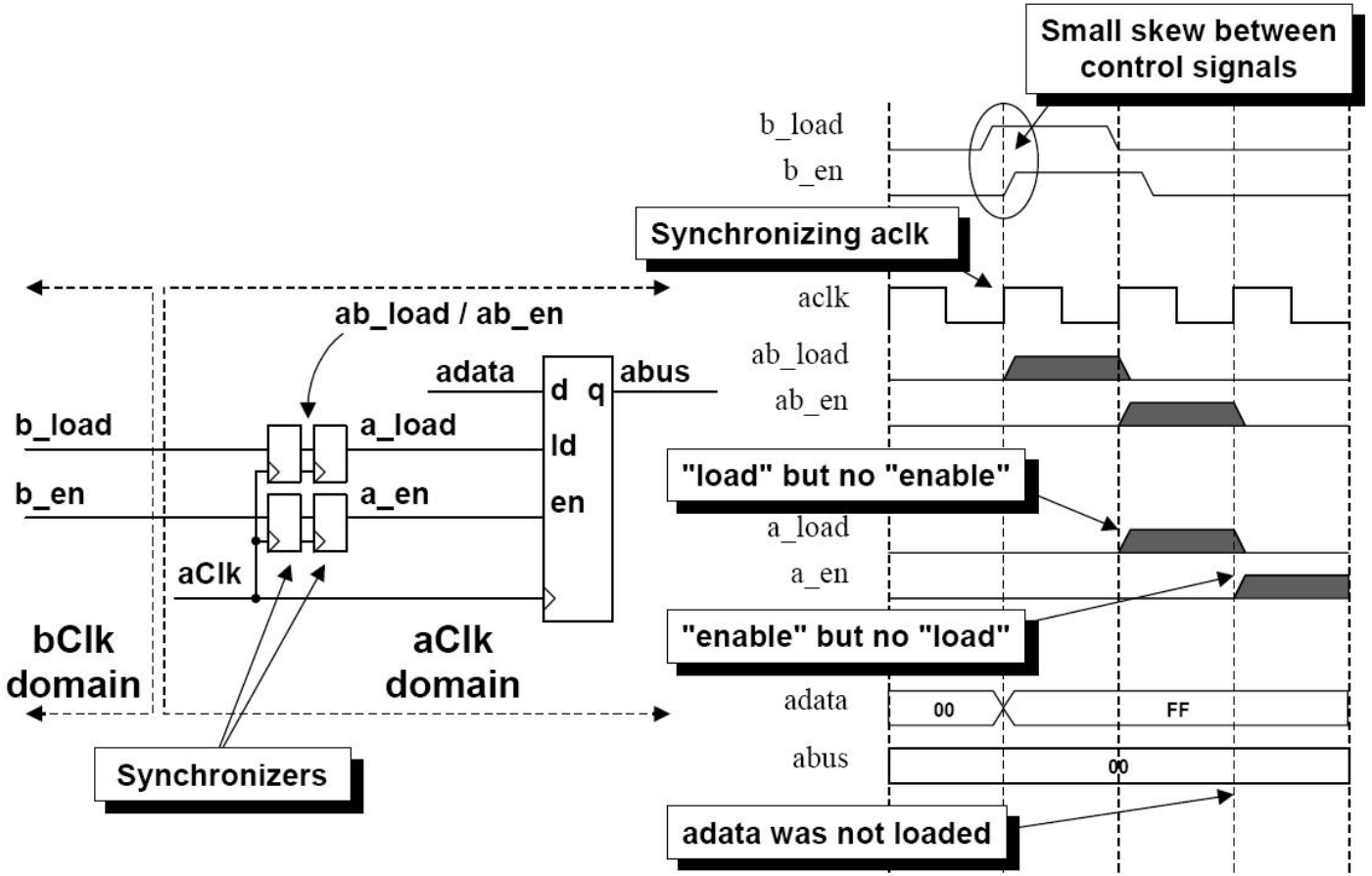


- Don’t have to consider the relation between clock periods
- Introduce significant delay due to the latency of the synchronizer

Source: Clifford Cummings, “Synthesis and Scripting Techniques for Designing Multi Asynchronous Clock Designs”

Passing Multiple Control Signals

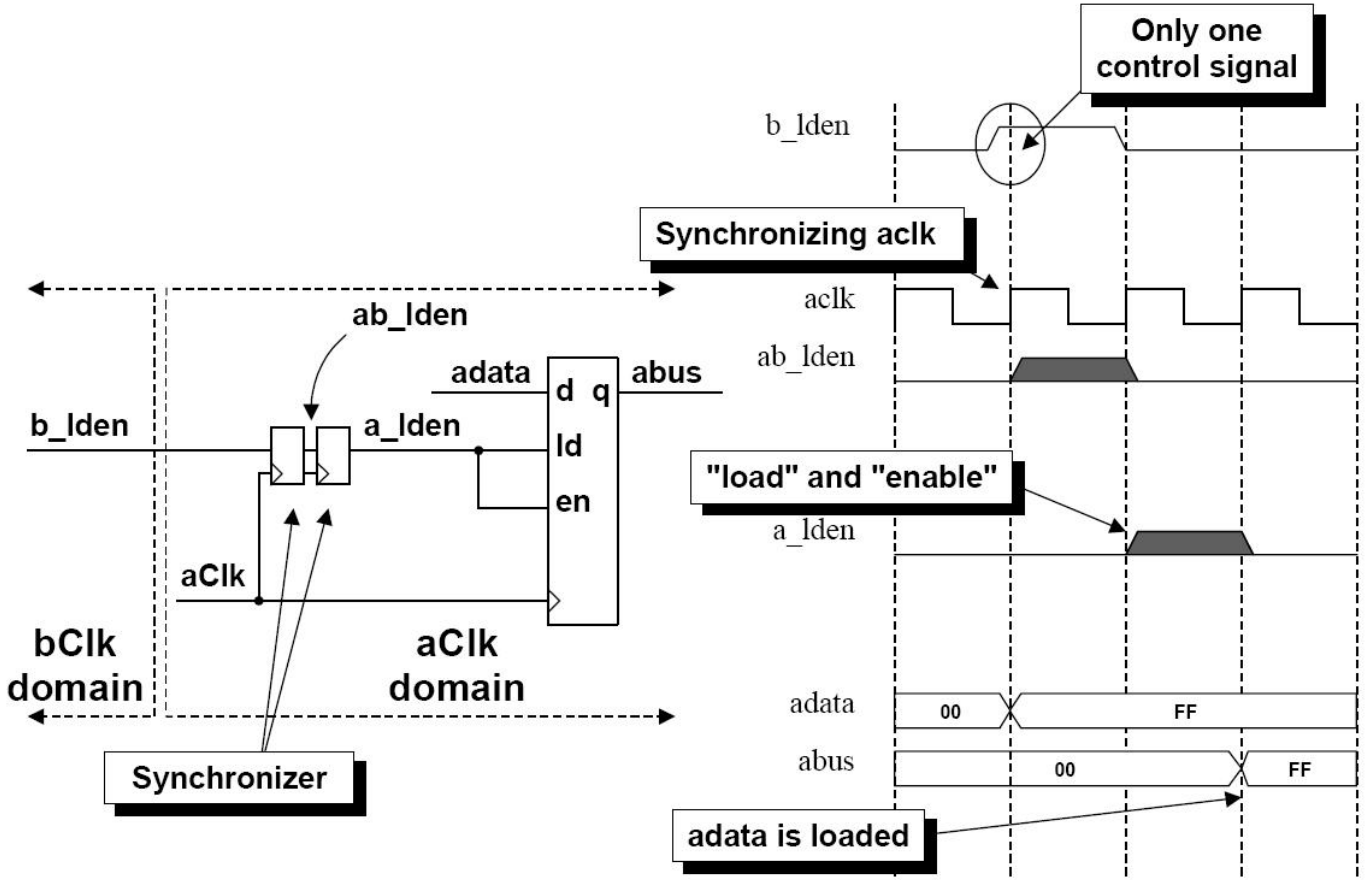
- CASE 1: two simultaneously required control signal



Source: Clifford Cummings, "Synthesis and Scripting Techniques for Designing Multi Asynchronous Clock Designs"

Passing Multiple Control Signals

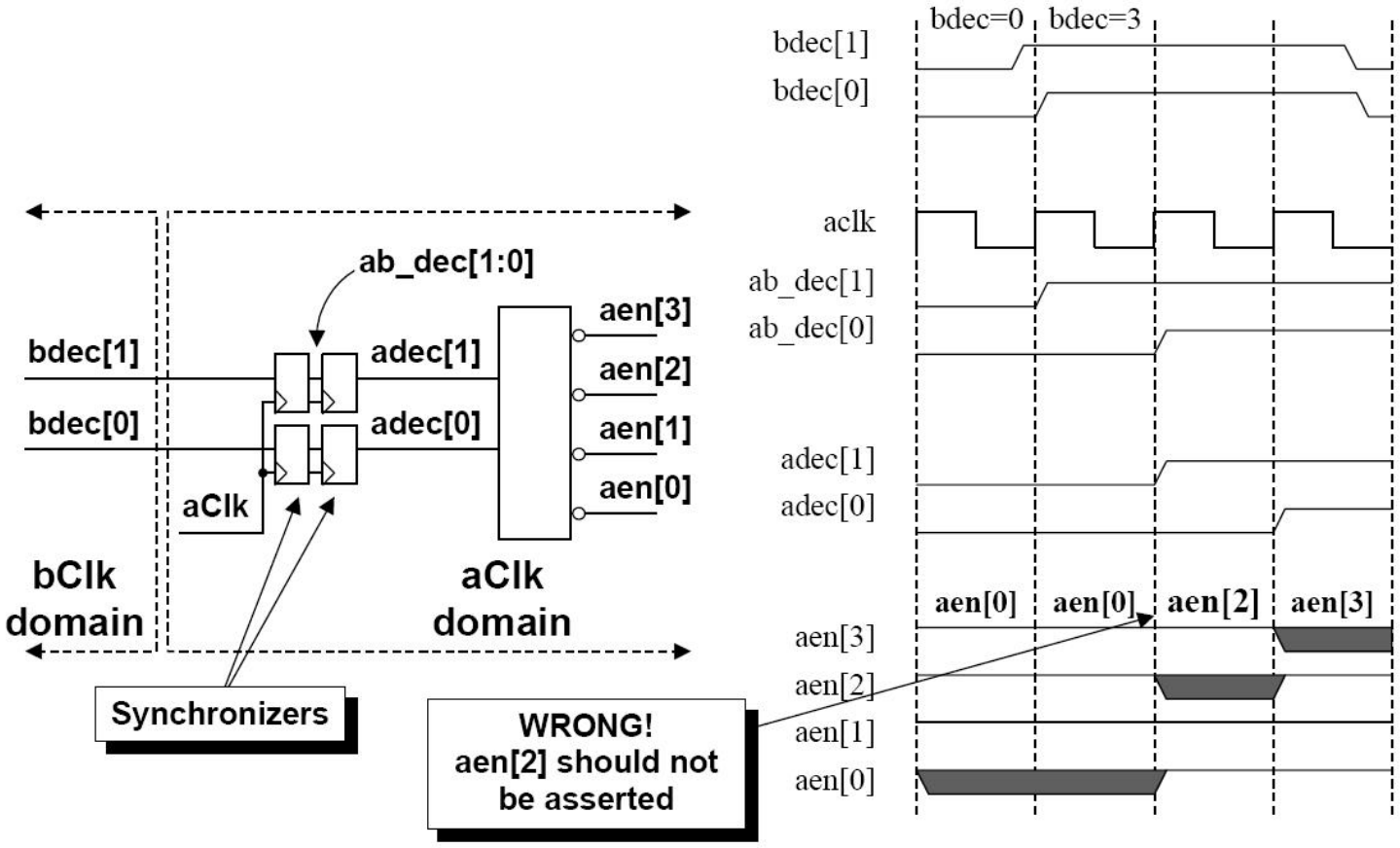
- Derived the two control signal from a single signal



Source: Clifford Cummings, "Synthesis and Scripting Techniques for Designing Multi Asynchronous Clock Designs"

Passing Multiple Control Signals

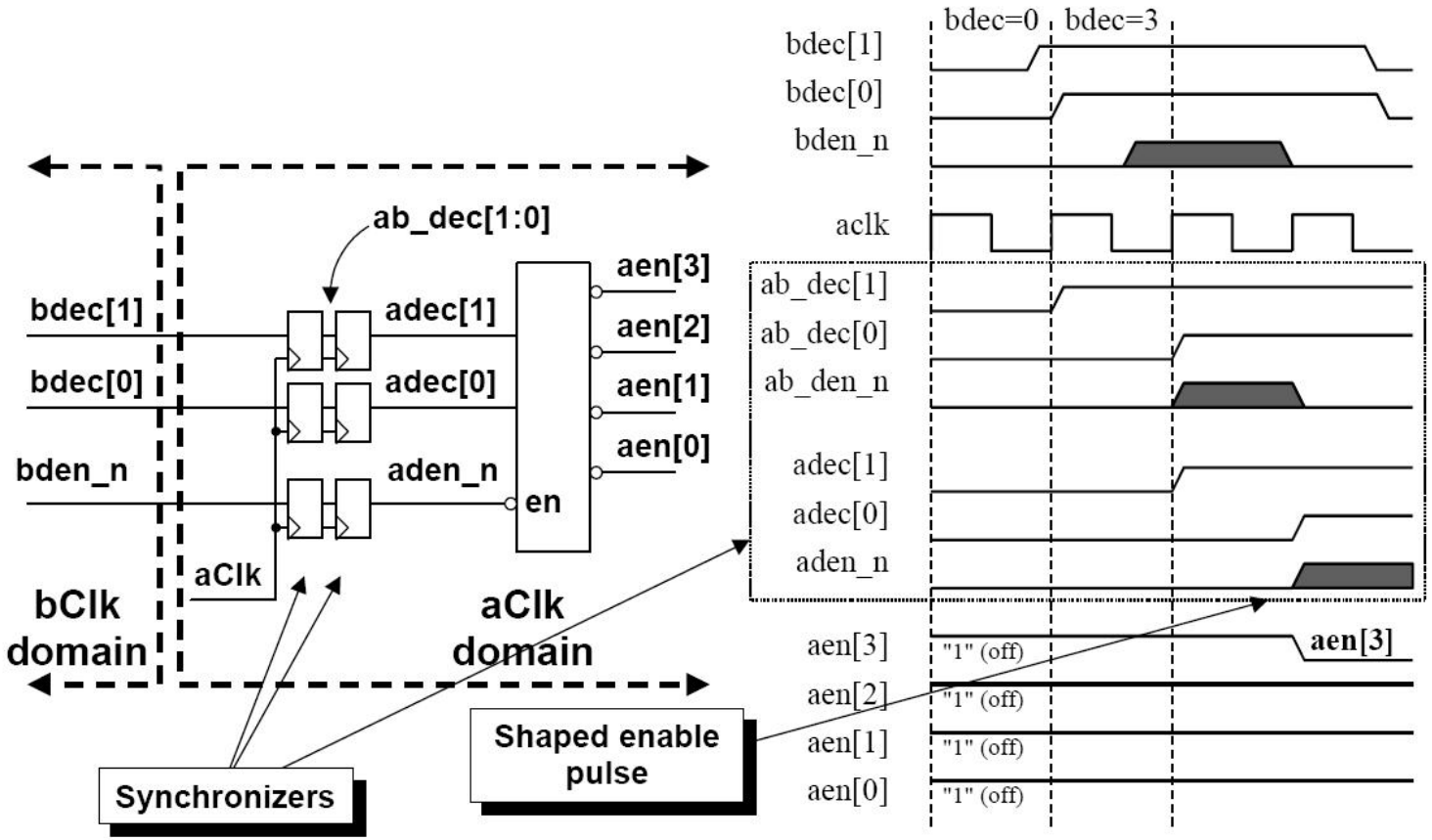
- CASE 2: two encoded signals



Source: Clifford Cummings, "Synthesis and Scripting Techniques for Designing Multi Asynchronous Clock Designs"

Passing Multiple Control Signals

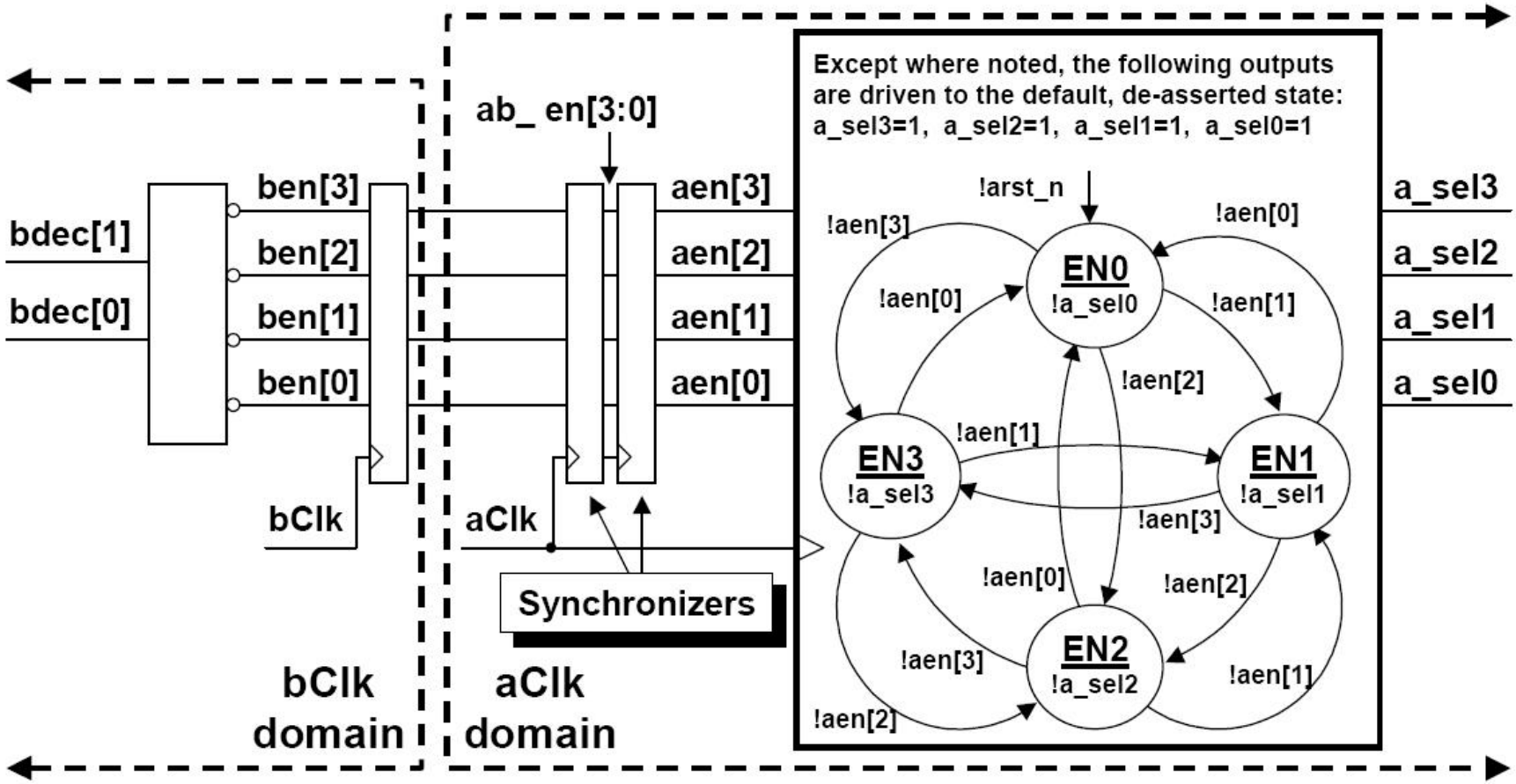
- Solution 1: added synchronized enable signal



Source: Clifford Cummings, "Synthesis and Scripting Techniques for Designing Multi Asynchronous Clock Designs"

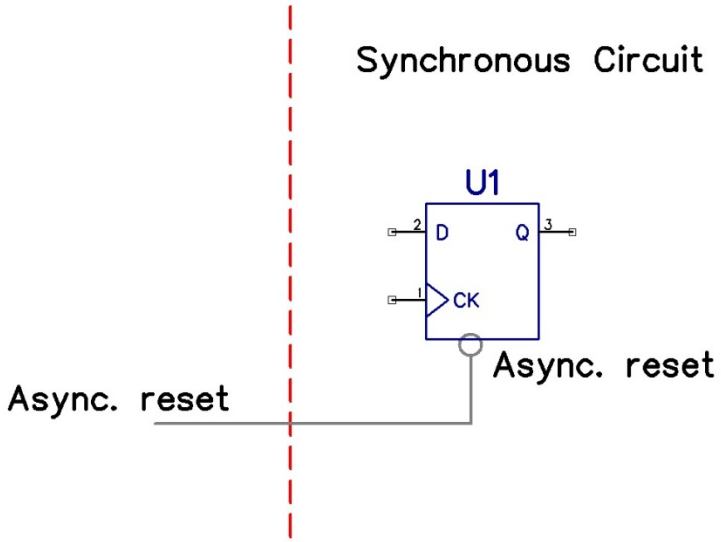
Passing Multiple Control Signals

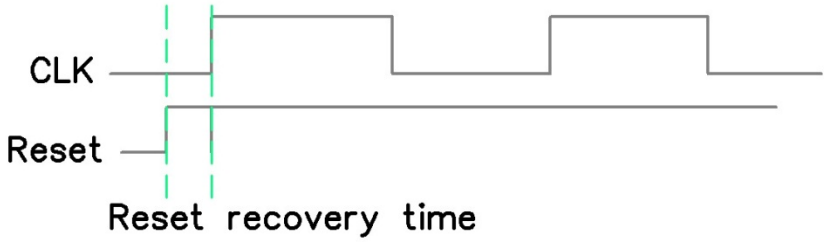
- Solution 2:

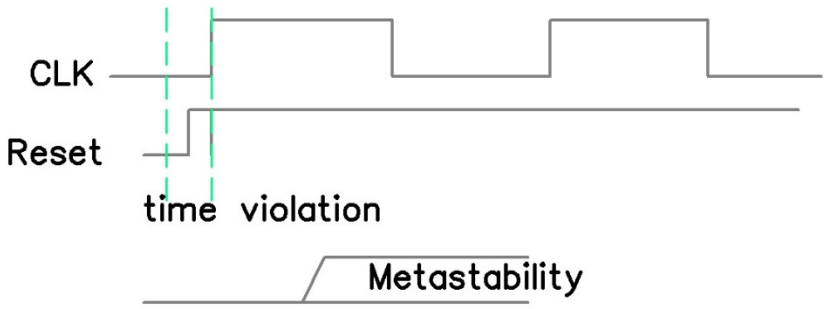


Source: Clifford Cummings, "Synthesis and Scripting Techniques for Designing Multi Asynchronous Clock Designs"

Asynchronous Reset/Set

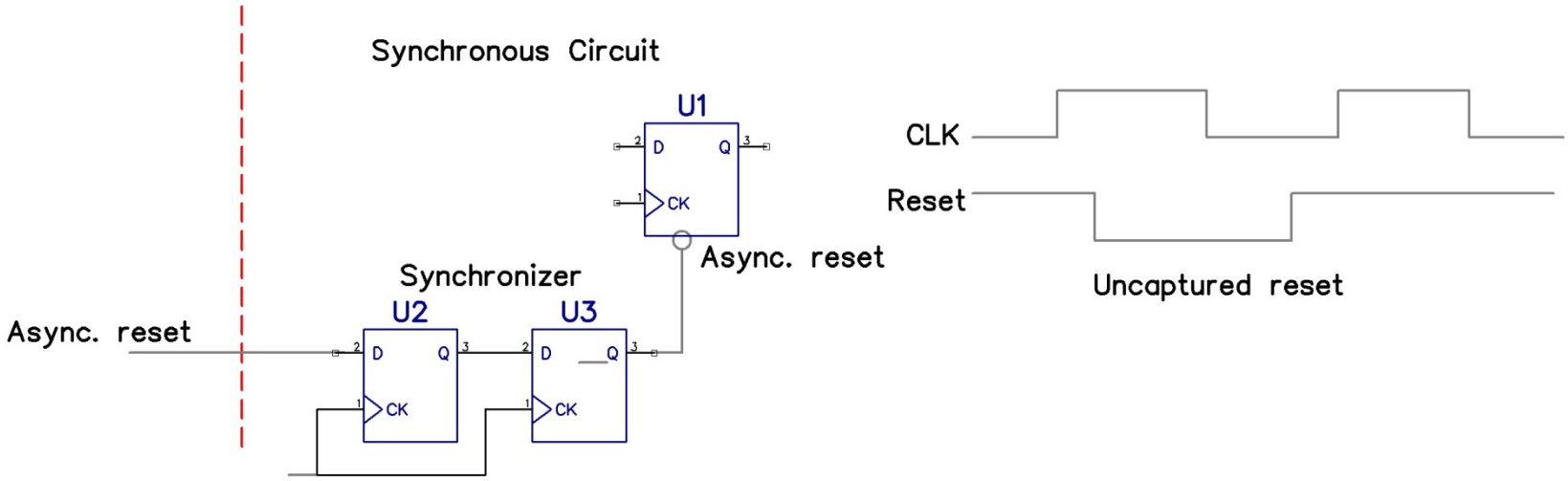






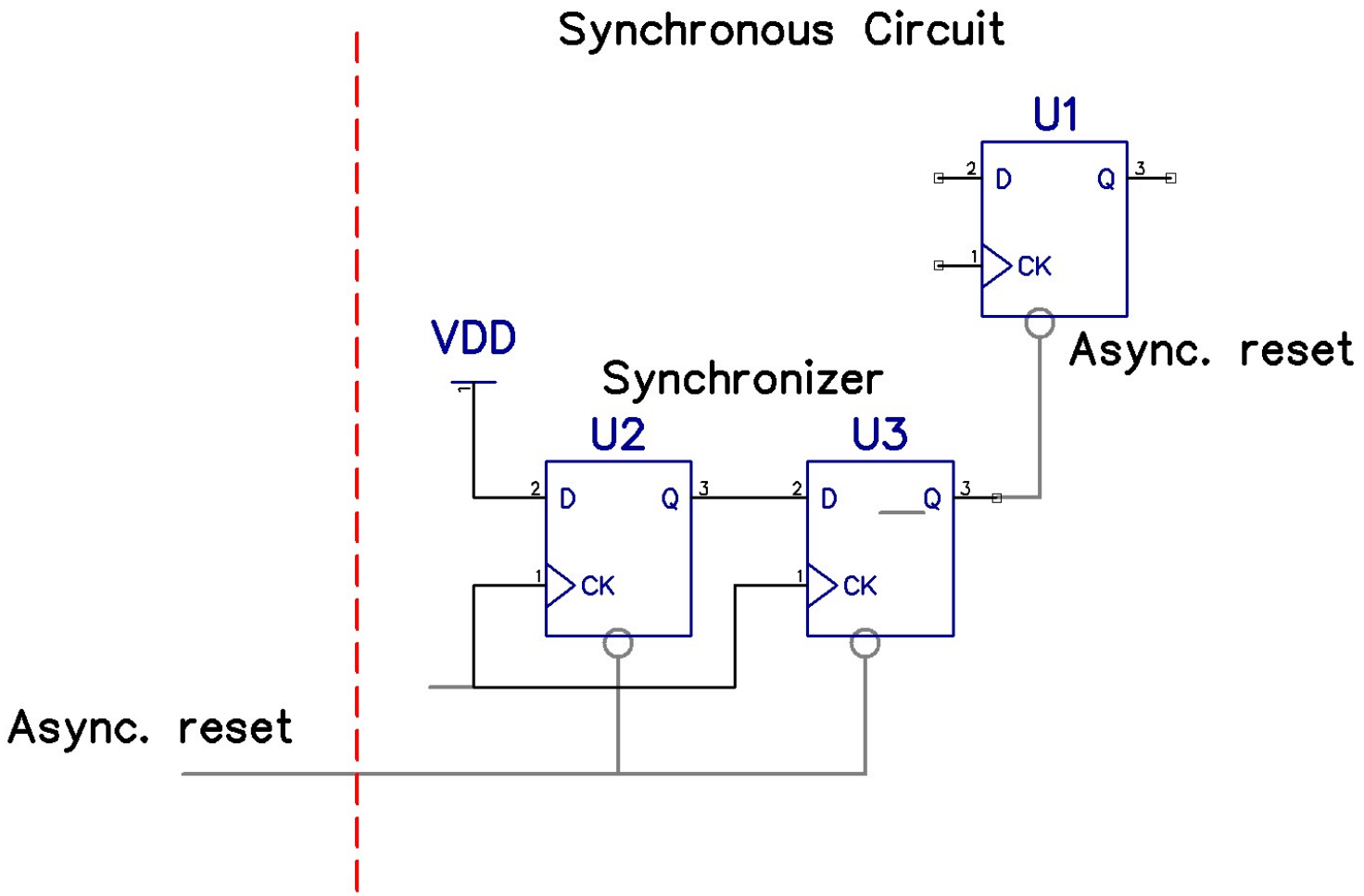
Source: Steve Kilts, "Advanced FPGA Design"

Synchronous Reset/Set



Source: Steve Kilts, "Advanced FPGA Design"

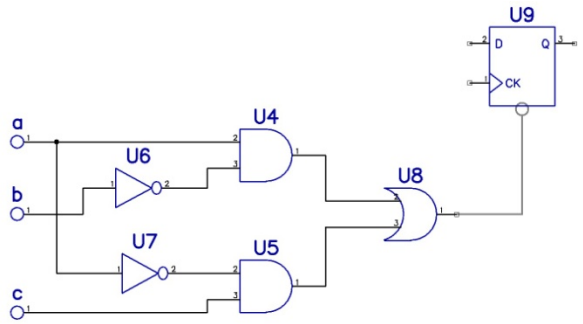
Asynchronous Assertion and Synchronous Desertion Reset/Set

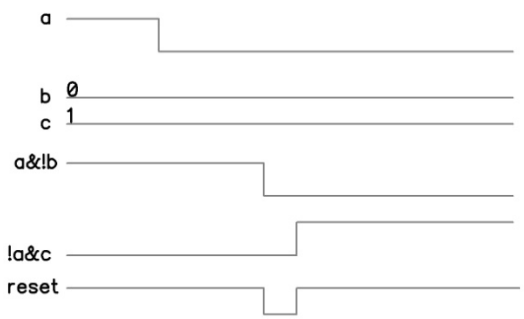


Source: Steve Kilts, "Advanced FPGA Design"

Internally Generated Reset/Set

- It is preferred to use synchronous reset/set if the reset/set signal is internally generated
- If asynchronous reset/set has to be used, need make sure the circuit that generates the reset/set signal is glitch free.





- Truth table of the reset logic

	00	01	10	11
0	0	0	1	0
1	1	1	1	0

- Adding a prime implicant

	00	01	10	11
0	0	0	1	0
1	1	1	1	0

Source: Steve Kilts, "Advanced FPGA Design"