Course Syllabus

Instructor: Haibo Wang, Room: ENGR E-116, Tel: 453-1522, zhwang@siu.edu
Office Hours: Monday, Wednesday and Friday 9:00 AM – 11:00 AM

If you have an early version of this book or the reference book, that will be fine. Lecture notes will be posted on Blackboard.


Course Time/Place:
Lecture: MWF 2:00PM - 2:50PM ENGR A-219

Course website: http://www.engr.siu.edu/~haibo/ece423

Course Description:
This course covers both fundamental and advanced topics in modern CMOS digital VLSI design. The topic include: brief introduction about MOS device characteristics and IC fabrication processes; IC layout techniques, design, characterization, and optimization of both combinational logic gates and sequential circuit elements, design of arithmetic and memory circuits. The course also discusses the new design challenges in on-chip interconnect, clock and power distribution network in modern VLSI. Labs and class projects will be given and account for a significant portion of the final grade. Cadence and Synopsys tools are the main CAD tools used in the class.

Topics:
1. MOS device characterizes
2. IC fabrication process
3. IC layout design
4. CMOS Inverter design and characteristics
5. Design of complex combination logic gates
6. Ratioed logic
7. Pass-transistor logic
8. Dynamic logic circuits
9. Latches and D flip-flops
10. Arithmetic circuits
11. Memory circuits
12. Interconnect challenges
13. Clock distribution challenges
14. Power distribution challenges
15. I/O circuits & ESD protection

Exam Schedule:
Midterm 1 9/26/11
Midterm 2 11/7/11
Final Exam 12/16/11
Grading Policy

Homework  5%
Labs      20%
Class Project  10%
Midterm 1  15%
Midterm 2   20%
Final Exam  30%


Class Policy:
1. No late homework, lab & project reports will be accepted except rare cases.
2. No early or makeup exams will be given except rare cases.
3. Rare cases are medical conditions (with Doctors’ notes), family emergency, and religious observations. Note that leaving school early for winter break is not qualified as a rare case.

Lab & Project
1. Six labs will be assigned. The objectives of the labs are listed below:
   o Lab 1: getting familiar with Cadence schematic capture, DC & transient analysis
   o Lab 2: getting familiar with layout design, LVS, and post-layout simulation
   o Lab 3: designing and optimizing the delay, power, and area of an inverter chain
   o Lab 4: designing and optimizing D flip-flops circuits
   o Lab 5: designing and optimizing dynamic logic circuits
   o Lab 6: designing and optimizing a full adder circuit
2. Class project: 4-bit X 4-bit array multiplier with carry-save circuit techniques.
3. Groups need to be formed to carry out labs and the project. Each group can at most have two students.

Blackboard Account:
You need blackboard account to check your grades and access class materials.