FPGA Programmable Interconnect and I/O Cells

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Definitions

- **Routing resources**: wires and switches (antifuse or pass transistors) that are used to transport signals in FPGA chips.

- **Routing Channels**: dedicated areas with fixed sizes that contain routing resources. Depending on wire directions in a routing channel, the channel can be called a horizontal channel or a vertical channel.

- **Track & Capacity**: a track holds one wire; the capacity of a routing channel is equal to the number of tracks it holds.
Antifuse Based Programmable Interconnect

- FPGA layout

- Realized connections
Antifuse Based Programmable Interconnect

- Since an antifuse takes a very small area, an antifuse can be implemented at every horizontal and vertical interconnect intersection. This type structure is called **fully populated**.

- The use of fully populated structures increase routing flexibility.

- Can not re-program.
Antifuse Based Programmable Interconnect

- The metal wires and antifuse contribute significant parasitic resistance and capacitance
- The parasitic resistance and capacitance result in large signal propagation delay and power consumption
- \[ \tau_{D4} = (R_1 + R_2 + R_3 + R_4)C_4 + (R_1 + R_2 + R_3)C_3 + (R_1 + R_2)C_2 + R_1C_1 \]
- \[ P_{dynamic} \propto (C_1 + C_2 + C_3 + C_4) \]
Programmable Interconnect Using Pass Transistors

- Pass transistors and their associated memories take large area. Thus, it is unrealistic to use fully populated structure.
- Normally, this type programmable interconnect has less routing flexibility.
- Can re-program.
Xilinx XC4000 Programmable Interconnect

Horizontal channel

Vertical channel

- Long wires
- Double length wires
- Single length wires
Xilinx XC4000 Switch Module

Switch Module

Connection example
Xilinx Programmable Interconnection Points

Routing channels

Programmable interconnection Point (PIP)

CLB

Double length wires

Single length wires

PIP

M
Xilinx XC4000 Programmable Interconnect

Connection example
FPGA Programmable I/O Cell

- I/O cells provide interface between internal FPGA circuits and external environment.
- An I/O cell can be configured as an input, output, or bidirectional port.
- D flip-flops are normally included in I/O cells to provided registered inputs and outputs.
Xilinx XC4000 Programmable I/O Cell
SelectIO Standard

- Allows direct connections to external signals of varied voltages and thresholds
  - Optimizes the speed/noise tradeoff
  - Saves having to place interface components onto your board
- Differential signaling standards
  - LVDS, BLVDS, ULVDS
  - LDT
  - LVPECL
- Single-ended I/O standards
  - LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
  - PCI-X at 133 MHz, PCI (3.3V at 33 MHz and 66 MHz)
  - GTL, GTLP
  - and more!

Source: Xilinx  Basic FPGA Architecture
Digital Controlled Impedance (DCI)

• DCI provides
  – Output drivers that match the impedance of the traces
  – On-chip termination for receivers and transmitters

• DCI advantages
  – Improves signal integrity by eliminating stub reflections
  – Reduces board routing complexity and component count by eliminating external resistors
  – Eliminates the effects of temperature, voltage, and process variations by using an internal feedback circuit

Source: Xilinx  Basic FPGA Architecture