Course Syllabus

Instructor: Haibo Wang, Room: ENGR E-116, Tel: 453-1522, zhwang@siu.edu
Office Hours: Tuesday and Thursday 2:00 PM - 4:00 PM, Monday 2:30-4:30PM


Xilinx User Manuals and Application Notes

Course Time/Place:
Lecture: Tuesday & Thursday 4:00AM - 5:15 AM ENGR A-208

Course website: http://www.engr.siu.edu/~haibo/ece428

Course Description:
The goal of the course is to introduce digital design techniques using field programmable gate arrays (FPGAs). We will discuss FPGA architecture, digital design flow using FPGAs, and other technologies associated with field programmable gate arrays. The course study will involve extensive lab projects to give students hands-on experience on designing digital systems on FPGA platforms.

Topics:
1. Introduction to ASICs and FPGAs
2. Fundamentals in digital IC design
3. FPGA & CPLD Architectures
4. FPGA Programming Technologies
5. FPGA Logic Cell Structures
6. FPGA Programmable Interconnect and I/O Ports
7. FPGA Implementation of Combinational Circuits
8. FPGA Sequential Circuits
10. Introduction to Verilog HDL and FPGA Design flow with using Verilog HDL
11. FPGA Arithmetic Circuits
12. FPGAs in DSP Applications
13. Design Case Study: Design of SDRAM Controller
14. Design Case Study: Design of Halftone Pixel Converter
15. Programming FPGAs in Electronic Systems
16. Design issues in complex systems containing both FPGA and Microprocessors

Exam Schedule:

<table>
<thead>
<tr>
<th>Exam</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Midterm 1</td>
<td>2/19/13</td>
</tr>
<tr>
<td>Midterm 2</td>
<td>4/9/13</td>
</tr>
<tr>
<td>Final Exam</td>
<td>5/9/13</td>
</tr>
</tbody>
</table>
Grading Policy

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework</td>
<td>10%</td>
</tr>
<tr>
<td>Labs</td>
<td>10%</td>
</tr>
<tr>
<td>Class Project</td>
<td>15%</td>
</tr>
<tr>
<td>Midterm 1</td>
<td>15%</td>
</tr>
<tr>
<td>Midterm 2</td>
<td>20%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>30%</td>
</tr>
</tbody>
</table>

A: 100-90,   B: 89-80,   C:79-70,   D:69-60,   F: <60

Class Policy:

1. No late homework, lab & project reports will be accepted except rare cases.
2. No early or make up exams will be given except rare cases.
3. Rare cases are medical conditions (with Doctors’ notes), family emergency, and religious observations. Note that leaving school early for winter break is not qualified as a rare case.

Lab & Project

1. Four labs will be assigned with focus on Xilinx ISE EDA tools, Spartan prototype board, how to use users constraints, arithmetic circuits.
2. A large design project will be assigned as the course project.
3. Groups need to be formed to carry out labs and the project. Each group can at most have two students.

Course online materials

Assignment, exam solutions and supplementary materials will be posted on Desire2learn.