ECE 327 LAB Introduction to XILINX Simulation

A project in ISE is a collection of all files necessary to create and download a design to the selected device. To create a new project for this tutorial:

Select File \rightarrow New Project.



In the **New Project** Wizard dialog box, give a Project Name as **Lab1** for Lab1. Type C:\tmp in the Project Location field. Select Schematic from the drop-down menu of Top-Level Module Type field. A schematic is a drawing that represents all or part of an electronic circuit

Project <u>N</u> ame:	Project Location:	
Lab1	c:\tmp\	
elect the type of Top-Level	module for the Project	
Top-Level Module Type:		
НП	<u>.</u>	
108 E		
HDL		
HDL Schematic EDIF		
HDL		

Click Next->Next.. Finish .

Select **Project -> New Source**



In the **New Source** wizard box select Schematic as shown. Then give a file name to your schematic and also the location in **Filename** and **Location** respectively.

) 📽 🖬 🗿 📴 🗑		ଞ୍ଚ ାହ ାଧାର ଜାଲା ସାହ ଜାଲା
ources in Project: Define Lab1 Cab 1 New S	Source	
Module View Module View M	P (CoreGen & Architecture Wizard) Schematic State Diagram Test Bench Waveform User Document Verilog Module	Eile Name: division2bit
rocesses for Source: "	Verilog Test Fixture VHDL Library VHDL Module VHDL Package VHDL Test Bench	Lo <u>c</u> ation:
		I ▲dd to project
C Process View	< <u>B</u> ack	ext > Cancel Help

This will open Engineering Capture System editor. **The Engineering Capture System** (**ECS**) is a graphical user interface (GUI) that allows you to create, view, and edit schematics and symbols for the Design Entry step of the Xilinx® design flow. The Schematic Editor mode of ECS allows you to open and edit schematic (SCH) files.

🚾 Xilinx ECS - [division2bit])(\mathbf{X}	- 🗆 🛛
K File Edit View Add Tools W	indow Help										- ć	×	
□ □ □ □ Image: Second	Ctrl+W Ctrl+D Ctrl+B Ctrl+G		€ © A	2.2	СЖ Ф Лt			ゴ 点 (無) /		8			
Options Symbols Symbol	Ctrl+F ne_Ctrl+1												
Select Opt Arc Circle When you click o Select the enl Rectangle C Select the line Text	Ctrl+L Ctrl+T	2	 		4	5	6		7			~	
 When you move an object Keep the connections to other objects Break the connections to other objects 	8											8	
When you use the area select tool, select the objects that	C 											C	
When you use the area select tool, select © Objects excluding attribute windows © Attribute windows only	division	2 2bit	3		4	5	6		1		8	-	
Change the editor to add symbol mode								[-:	34,96	2] v	irtex	2 //	

Click Add -> Symbol.

This wll open the Symbol Editor. The Symbol Editor mode of ECS allows you to open and edit symbol (SYM) files. Symbols are the basic elements of a schematic.

To place a 2-input AND gate, type **and2** in the **Symbol Name Filter** field. It gives all the gates whose name starting with **and2**. Select **and2** and place it on the editor(White Space) as shown below. Select required gates according to your circuit.



After placing the gates, you have to connect the gates. You can do this using **wire**. Click **Add->Wire**.

🚾 Xilinx ECS - [di	vision2bit]																					-		
👗 File Edit View	Add Tools Win	dow	Hel	р																			- 0	x E
	Wire	Ctrl	+W		-	ri I	G) (Ð	4	• 3	έđ	圖)	¢			2	5	5	l E	1		-	
<u> </u> र रा क्ष्ट क्ष	Net Name Bus Tap I/O Marker	Ctrl Ctrl Ctrl	+D +B +G] A	1	?		ç,	AIP.		/		k i	= . ₽,		L Z	. 1				
Options Symbols	Symbol Instance Name	Ctrl Ctrl	+F +J																					
No Optio	Arc Circle					2	1		3	1		4	L	5		T	6	_	1	7		1	В	
	🗸 Line	Ctrl	+L		÷.		10	•	•		22		•	•	e.	1	•3	10		•		22	10	
	Rectangle				÷.	15	10	1	÷	1	10	10		30		1	6 ji	18	30	×	1	20	10	A
	Text	Ctrl	+T		÷.	-	12	•		24	24	- 2				24	•	13		14	24	33	13	
1		F	40	1	4	22		S.	×.	4	8 4)÷	Si.	1	4	20	•	Si.	ŝ.	4	8 8		
			1	12		:33	•	1	3	22	2	-	•	1	2	-	- 9	13	1	3	22	22	13	
			12		1		10		•	1	22		•			2	7	10			1	22	10	
				1	1	-84	13	•	÷	3	1	-				3	-81	8	•	\cdot	10	1	8	
				•	24	•	•	•	•	24	34 -	1	-	•	•	24	•	•	•		24		-5	
				2	•	. 22	•			•	۰.	•	•			•	•	•		•	•	S.	1	

And connect the terminals of the gates as shown.



To apply the signals, you must have pins at the terminals of gates. You can place pins by clicking **Add->I/O Marker** as shown.

🚾 Xilinx ECS - [div	rision2bit]																					-		X
🗙 File Edit View	Add Tools Win	ndow	He	P																			- t	5 ×
」D 2 ਹਿ ਹੈ €] ੮ ਹੀ ਘੁੰ ਘੁੰ	Wire Net Name Bus Tap ✔ I/O Marker	Ctr Ctr Ctr	+W +D +B +G]]@] /		Э , [?	X] (;); ;);	€ (⊿ ⊾		¢				_` _		.	5	3		
Options Symbols	Symbol Instance Name	Ctr Ctr	1+F 1+J																					_
Add I/O Marker	Arc Circle					2	Ť	3	3	T			1	5	2	ĺ.	6		1	7			8	
When you click n end of a branch, you want to do?	Line Rectangle Text	Ctr Ctr	1+L 1+T		•		1	•	12 12 12	5 5 5	5 7 8	1	• • •		1. 10	10 10 10 10 10			• • •	10 10 10	•	3		*
C Add an output C Add a bidirection	marker onal	-	•	•		а С	64 85	12	•3 20	*	ti S	P) <u>.</u>	÷.	14 12	•	•	19 19	•	•3 23	•			
marker C Remove the ma	arker	В	10 IS	• • •		:			12 12 12	•		÷			•	÷ .	- - -	•		12 12	• • •	• • •		В
When you add an marker, set its orier	I/O ntation so	-		2 1	N. 8. 3			10 C 10		1		1	•		1. 12	2 N	14 14	1	10.00	9. 20	. ×			



Change the name of pins by right-clicking pin and select **Object properties.** Change the Name field to required name. If it is a **A** input change name to **A**.

🗙 File Edit View Add Tools Win	low Help	- 8 ×
	▶ ~ 囲	
K J ♥ ♥ ► ਙ \$ #	ヽ o ヽ □ A ヱ ♀ ₄ ✔ ★ ★ ★ ★	
Options Symbols		
Select Options		
When you click on a branch © Select the entire branch © Select the line segment	Cut Copy Paste Delete	
When you move an object Keep the connections to other objects Break the connections 	Zoom Zoom Select Object(s) Select All Unselect All	• • •
When you use the area	Mirror	
select tool, select the objects that	Object Properties	· · ·

Then in main window(Project Navigator) double-click the Synthesize-XST as shown.

ile Edit '	view Pri	oject	Sour	rce	Proces	is V	Vindo	w H	lelp		0.0
	8		1		E.	C	3	P		A	ę
· ·	D · · ·						_	-×			i
Sources in	Project:							_			
	2v40-4cs1	144									
•	division	2bit (di	vision	2bit.s	ch)						
-											
Madul	o View	Car	anahot	View	A	Librar	v Mieu		1		
-G Modul	e View	🗖 Sna	apshot	: View	D	Librar	y Vieu	v	J		
- C Modul	le View 🛛	ta Sna	apshot	t View		Librar	y Vieu	v A ×	- -		
Processes	le View	to Sna ce: "di	apshot visior	t View n2bit''		Librar	y Vieu	v L×			
Processes	for Source	te: "di xisting	apshot vision Sour	t View 12bit''		Librar	y Vieu				
Processes	for Source Add E Create	te: "di xisting New	vision Sour	t View 12bit'' ce ce		Librar	y Vieu	v ••×			
Processes	for Source Add E Create Design	te: "di xisting New n Entry	vision Sour Sour	t View n2bit'' ce ce ies		Librar	y Vieu				
Processes	for Source Add E Create Design User C	te: "di xisting New n Entry Constra	vision Sour Sourc Utiliti	t View n2bit'' ce ce ies		Librar	y Vieu	v A ×			
Processes	for Source Add E Create Design User C Synthe	ce: "di xisting New n Entry Constra	vision Sour Sour Utiliti aints XST	t View n2bit'' ce ce ies		Librar	y Vieu				
Processes	for Source Add E Create Design User C Synthe Implen	ce: "di xisting New n Entry Constra esize - nent D	vision Sour Sour Utiliti aints ×ST esign	t View n2bit'' ce ce ies		Librar	y Vieu				
Processes	for Source Add E Create Design User C Synthe Implen Gener	ce: "di xisting New n Entry Constra esize nent D ate Pro	vision Sour Sour Utiliti aints ×ST esign ogram	t View n2bit'' ce ce ies	File	Librar	y Vieu				
Processes	for Source Add E Create Design User C Synthe Implen Gener	ce: "di xisting New n Entry Constra esize nent D ate Pro	vision Sourc Ottiliti XST esign ogram	12bit'' ce ies	File	Librar	y Viev				
Processes	for Source Add E Create Design User C Synthe Implen Gener	ce: "di xisting New n Entry Constra esize nent D ate Pro	visior Sour Sour Utiliti sints XST esign	t View n2bit'' ce ce ies nming	File	Librar	y Vieu	υ • ×			
Processes	for Source Add E Create Design User C Synthe Implen Gener	Sna ce: "di xisting a New n Entry Constra esize nent D ate Pro	visior Sour Sour Utiliti sints ×ST esign ogram	t View n2bit'' ce ce ies	File	Librar	y Vieu				
Processes	for Source Add E Create Design User C Synthe Implen Gener	Sna xisting New n Entry Constra esize nent D ate Pro	visior Sour Sour Utiliti sints XST esign ogram	t View 22bit" ce ce ies	File	Librar	y Vieu				

If everything is correct, go to Add->New Source. In the New Source wizard box click **Test Bench Waveform.** After synthesizing, you have to apply the inputs. You can do this using a special file called Test Bench file. In this file you mention the required inputs to your circuit.

Give a name to your test bench file and also location as earlier.

New Source	
BMM File Implementation Constraint: File Implementation & Architecture Wizarc) MEM File	File Name:
Schematic	divisiontest
 State Diagram ✓ Test Bench Waveform 	Location:
User Document	c:\tmp
Verling Module Verling Test Fixture VHDL Libiary VHDL Module VHDL Package VHDL Test Bench	
1	🔽 Acd to project
2	
K Back Next >	Cancel Help

A window will pop up asking the interval of inputs. Leave it as it for now.

itialize Timing		2
Preview		
Assign Inputs	Check Outputs	Assign Inputs
	ait To neck	Nait To Assign ➡
Clock Timing Inputs are assigned at 'input se outputs are checked at 'outpu Rising Edge C Fall Dual Edge (DDR or DET	etup time' and t valid delay'. Ing Edge design]	ype gle Clock D V tiple Clocks nbinatorial Design (or internal clock)
Clock high time 100	ns Combinat	orial Timing
Clock low time 100	ns Inputs are checked.	assigned, outputs are decoded then A delay between inputs and outputs
Include a structure 100	avoids ass	signment/checking conflicts.
Input setup time 10	ns avoids as:	signment/checking conflicts.
Input setup time 10 Output valid delay 10 Offset 0	ns avoids as: ns Check out ns Assign inp	tputs 50 ns after assign inputs
Input setup time 10 Output valid delay 10 Offset 0 Global Signals (Verilog Only) -	ns avoids as: ns Check out ns Assign inp Time S	signment/checking conflicts. tputs 50 ns after assign inputs uts 50 ns after output cale ns
Input setup time 10 Output valid delay 10 Offset 0 Global Signals (Verilog Only) – PRLD (CPLD) GS	ns Assign inp	signment/checking conflicts. tputs 50 ns after assign inputs uts 50 ns after output cale ns v

Click OK.

Then select requird inputs as shown. Then save your file. Then click **Generate Expected Simulation Results** on left hand side as shown.

