ECE 428 Programmable ASIC Design

CPLD and FPGA Architectures

Haibo Wang
ECE Department
Southern Illinois University
Carbondale, IL 62901

Definitions

- Field Programmable Device (FPD):

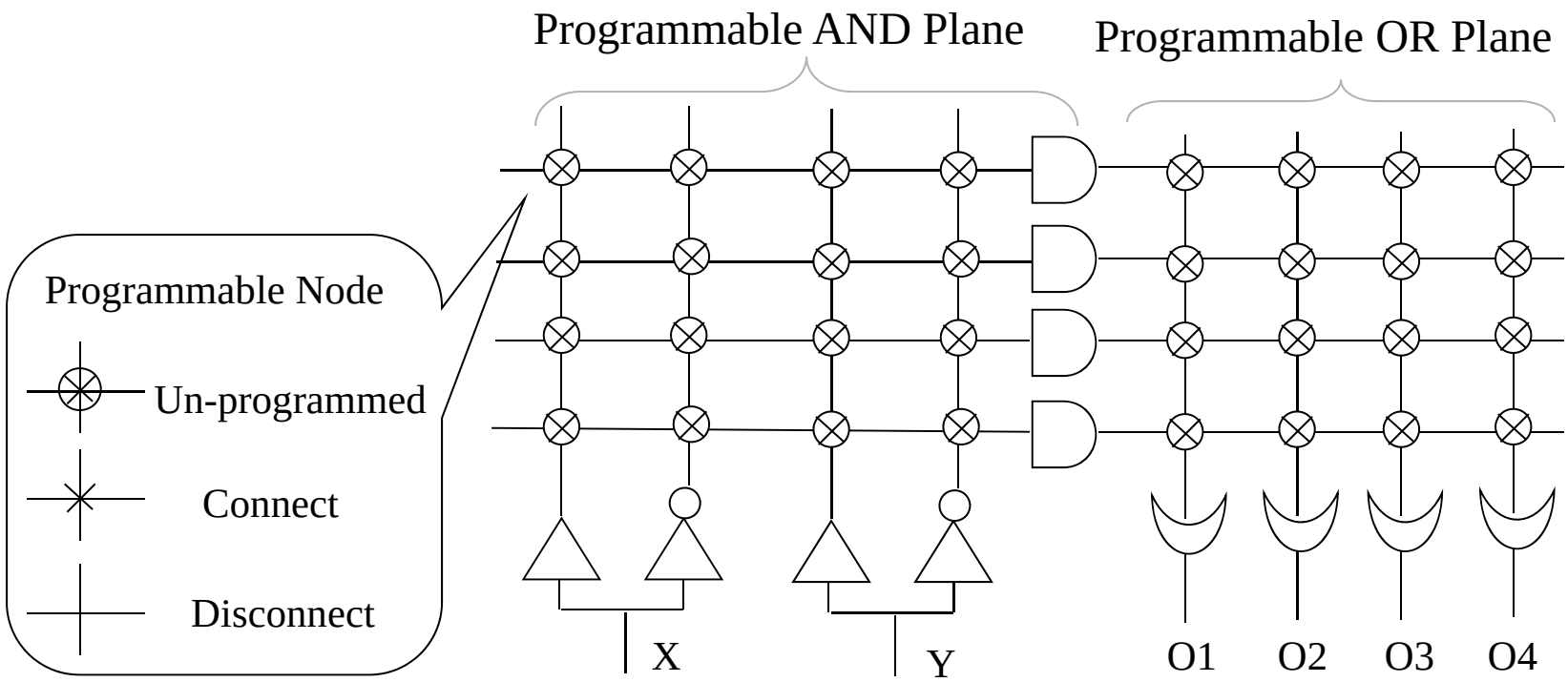
  — a general term that refers to any type of integrated circuit used for implementing digital hardware, where the chip can be configured by the end user to realize different designs. Programming of such a device often involves placing the chip into a special programming unit, but some chips can also be configured “in-system”. Another name for FPDs is *programmable logic devices* (PLDs).

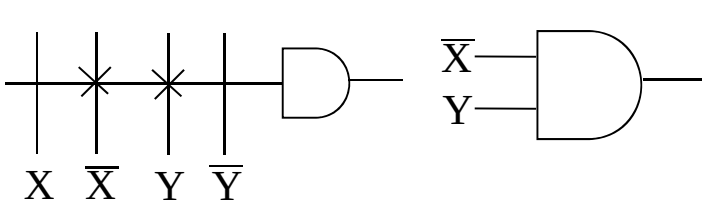
Source: S. Brown and J. Rose, FPGA and CPLD Architectures: A Tutorial, IEEE Design and Test of Computer, 1996

Classifications

- ***PLA*** — a Programmable Logic Array (PLA) is a relatively small FPD that contains two levels of logic, an AND-plane and an OR-plane, where both levels are programmable
- ***PAL*** — a Programmable Array Logic (PAL) is a relatively small FPD that has a programmable AND-plane followed by a fixed OR-plane
- ***SPLD*** — refers to any type of Simple PLD, usually either a PLA or PAL
- ***CPLD*** — a more Complex PLD that consists of an arrangement of multiple SPLD-like blocks on a single chip.
- ***FPGA*** — a Field-Programmable Gate Array is an FPD featuring a general structure that allows very high logic capacity.

PLA


Programmable AND Plane
Programmable OR Plane
Programmable Node
Un-programmed
Connect
Disconnect
X
Y
O1
O2
O3
O4


X
$\overline{X}$
Y
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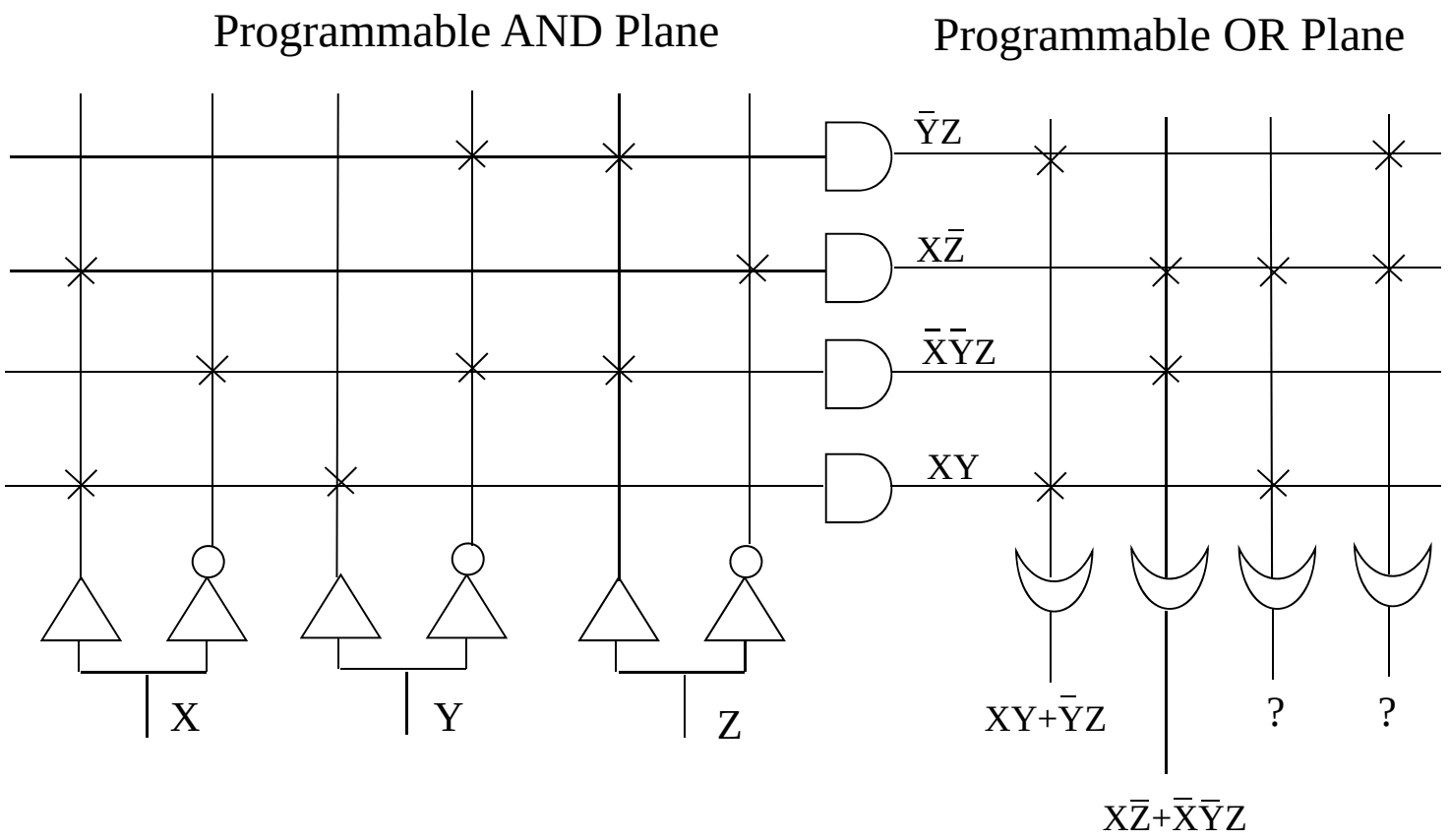
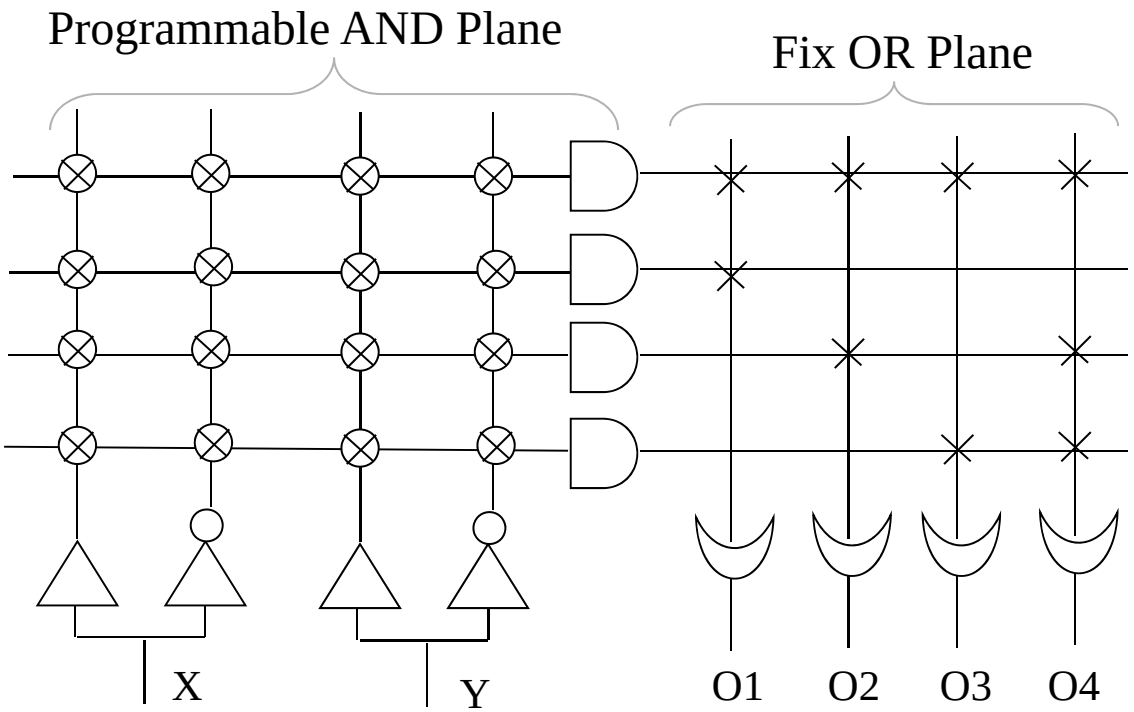
$\overline{X}$
Y
X$\overline{Y}$
$\overline{X}$Y
X$\overline{Y}$
$\overline{X}$Y

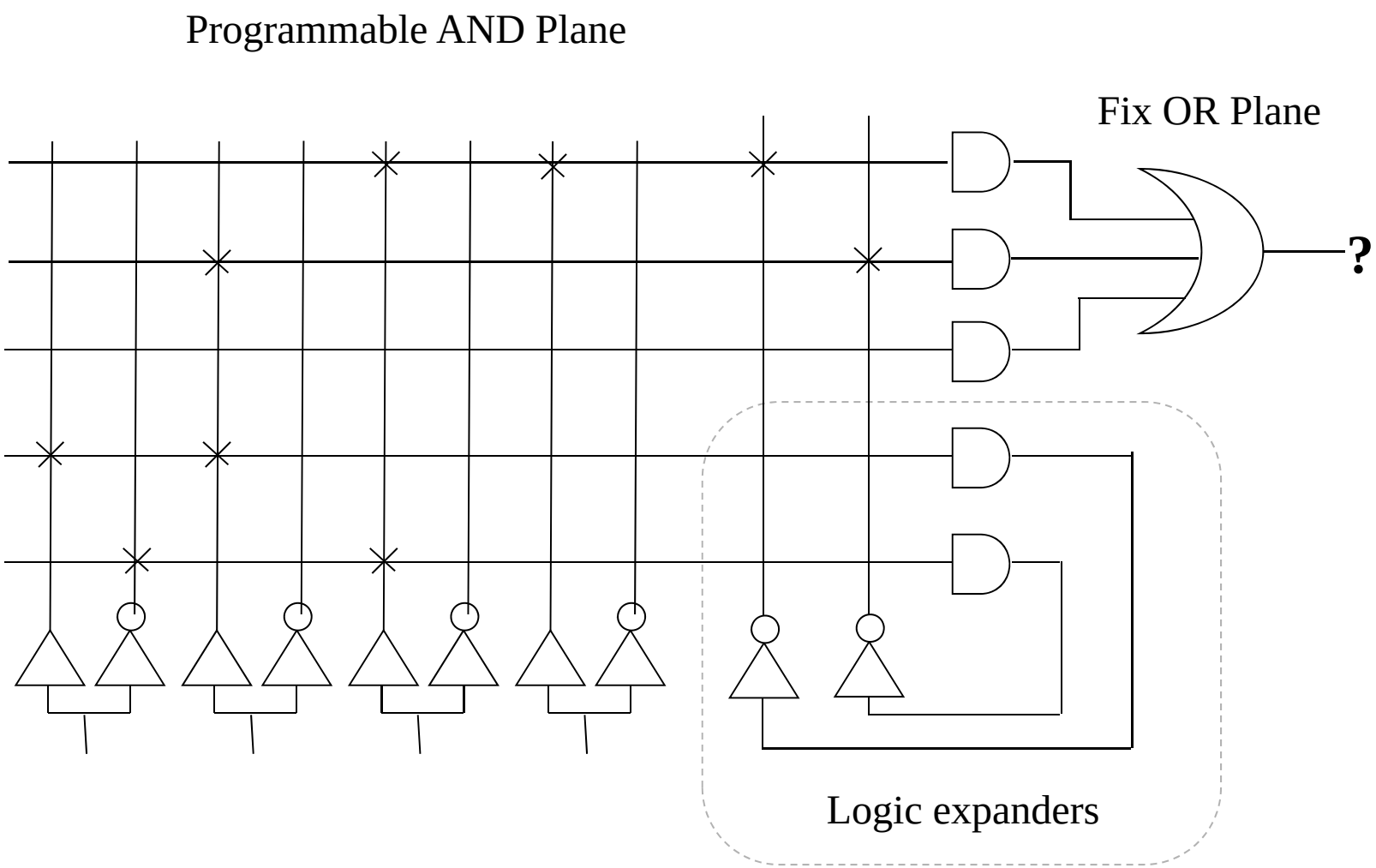
PLA


Programmable AND Plane
Programmable OR Plane
$\bar{Y}Z$
$X\bar{Z}$
$\bar{X}\bar{Y}Z$
XY
X
Y
Z
$XY+\bar{Y}Z$
?
?
$X\bar{Z}+\bar{X}\bar{Y}Z$

PAL



PAL with Logic Expanders

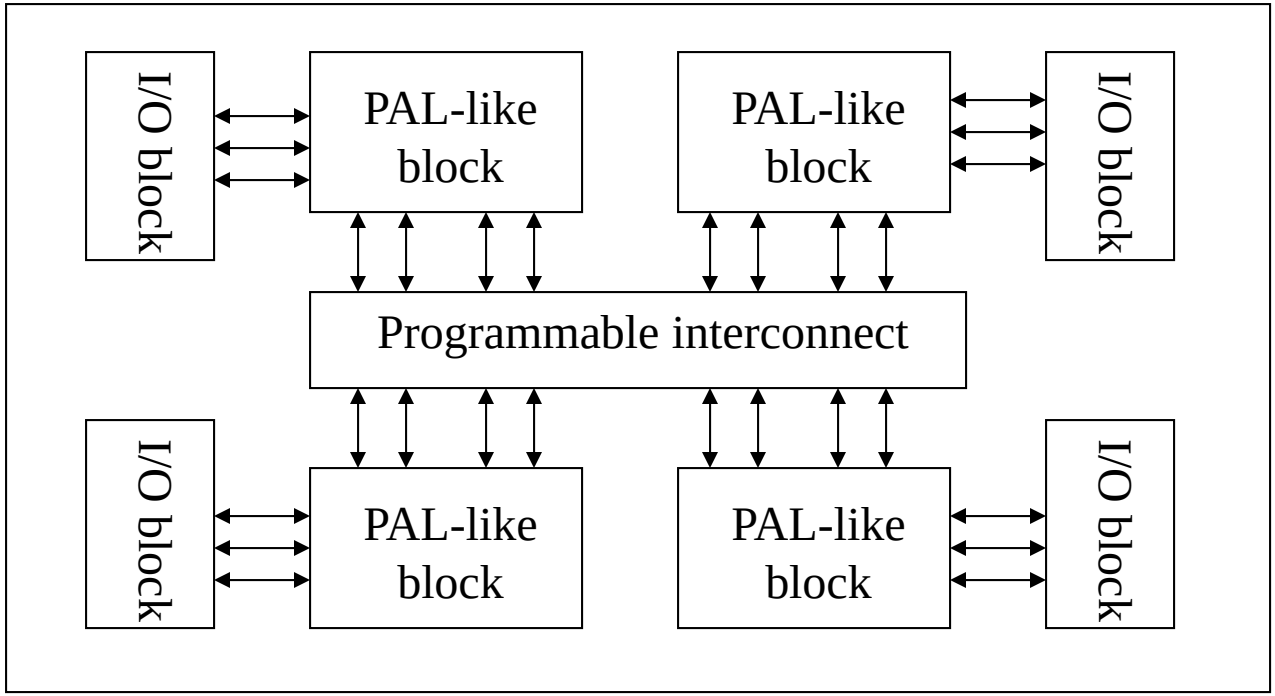


PLA *v.s.* PAL

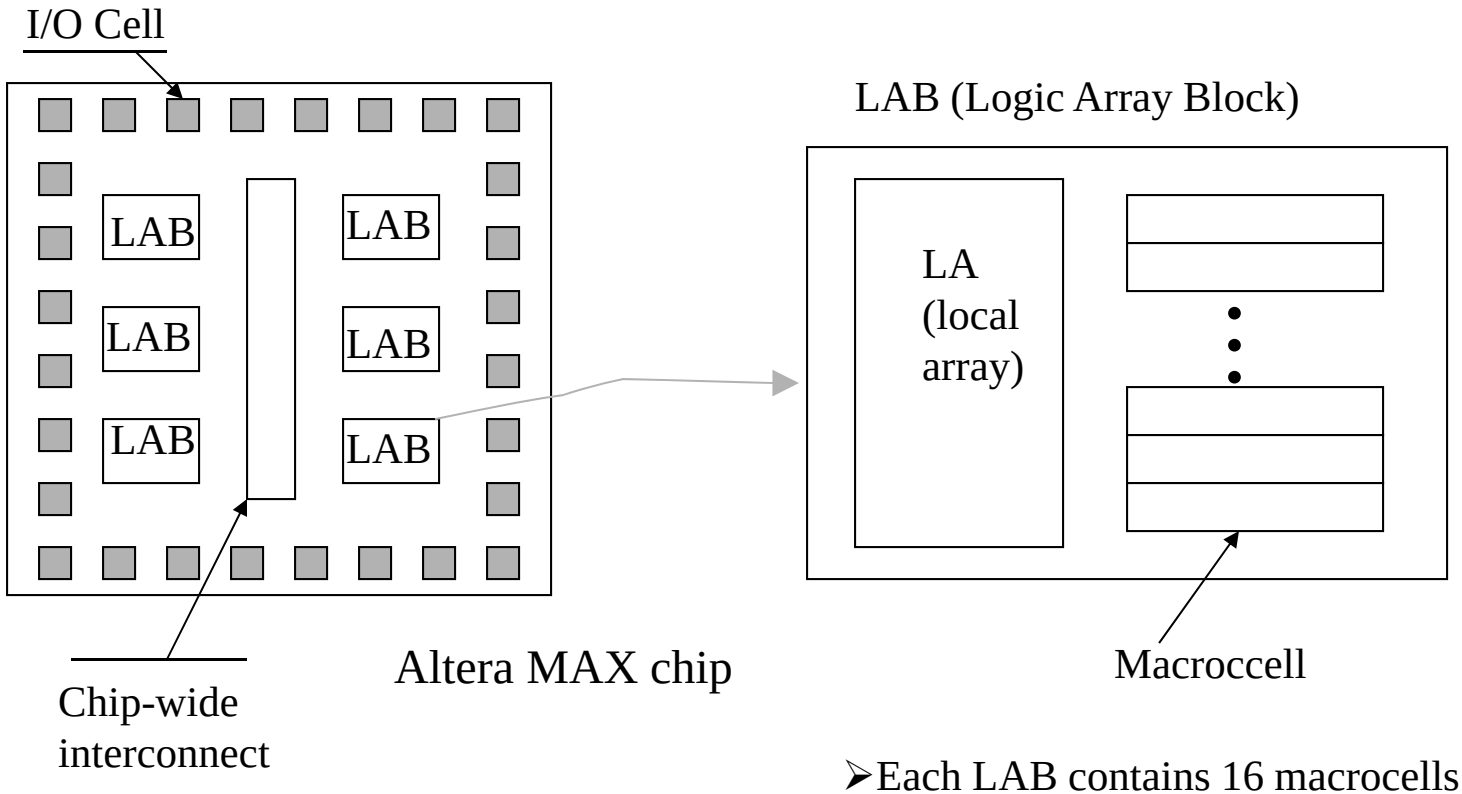
- PLAs are more flexible than PALs since both AND & OR planes are programmable in PLAs.
- Because both AND & OR planes are programmable, PLAs are expensive to fabricate and have large propagation delay.
- By using fix OR gates, PALs are cheaper and faster than PLAs.
- Logic expanders increase the flexibilities of PALs, but result in significant propagation delay.
- PALs usually contain D flip-flops connected to the outputs of OR gates to implement sequential circuits.
- PLAs and PALs are usually referred to as SPLD.

CPLD

- A CPLD comprises multiple PAL-like blocks on a single chip with programmable interconnect to connect the blocks.
- CPLD Architecture

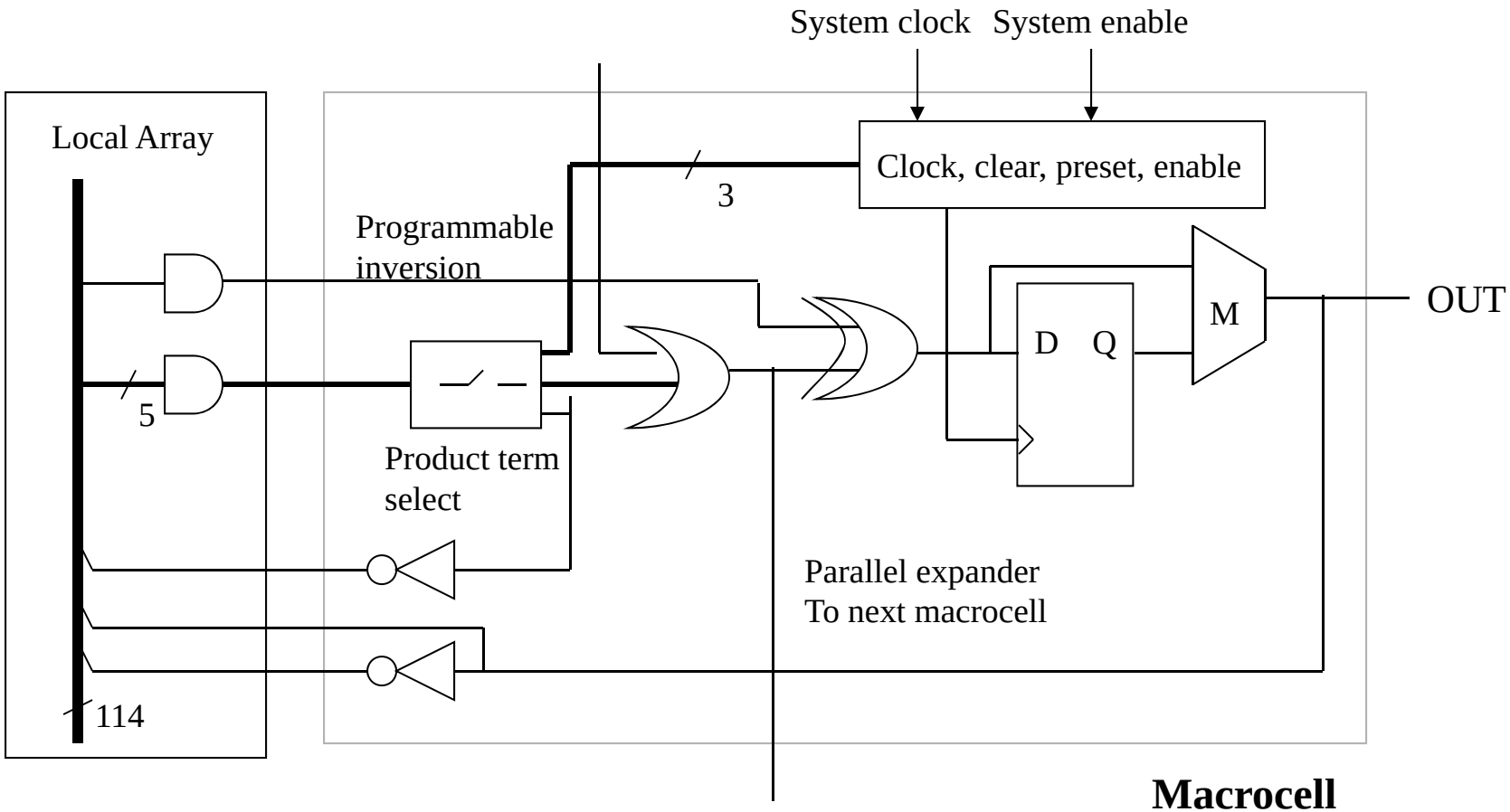


Altera MAX CPLD



➢Each LAB contains 16 macrocells

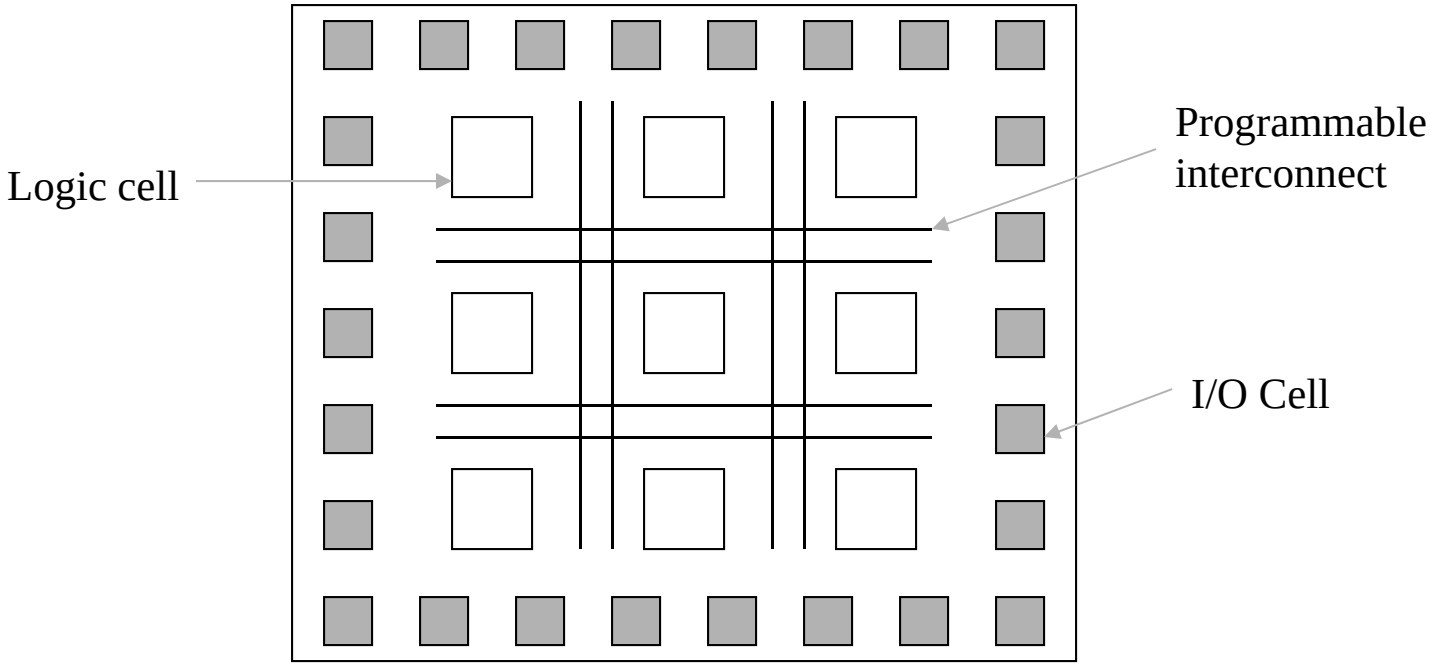
Macrocell of Altera MAX CPLD



MAX 9000 has 33 inputs, can you explain why LA has 114 inputs?

FPGA

- FPGA consists of an array of programmable basic logic cells surrounded by programmable interconnect.
- FPGA Structure



FPGA *v.s.* CPLD

- Capacitance

	SPLDs	CPLDs	FPGAs
Equivalent gates	0 ~ 200	200 ~ 12,000	1000 ~ 1,000,000

- Applications

CPLDs	FPGAs
1. Implement random glue logics or Replace circuits previously implemented by multiple SPLDs 2. Circuits that can exploit wide AND/OR gates, and do not need a very large number of flip-flops are good candidates for implementation in CPLDs.	1. FPGAs can be used in various applications: prototyping, FPGA-based computers, on-site hardware re-configuration, DSP, logic emulation, network components, etc.