# FPGA Logic Cells and Architecture

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Overview

❑ An FPGA contains a large number of logic cells. Each logic cell can be configured to implement a certain set of functions.

❑ Each logic cell has a fixed number of inputs and outputs.

❑ Logic cells used in FPGAs

— Multiplexer based logic cells (e.g. Actel FPGAs)

— Memory based logic cells (e.g. Xilinx FPGAs)

Multiplexer Based Logic Cells

❑ A multiplexer-based logic module is typically composed of a tree of 2-to-1 MUXes
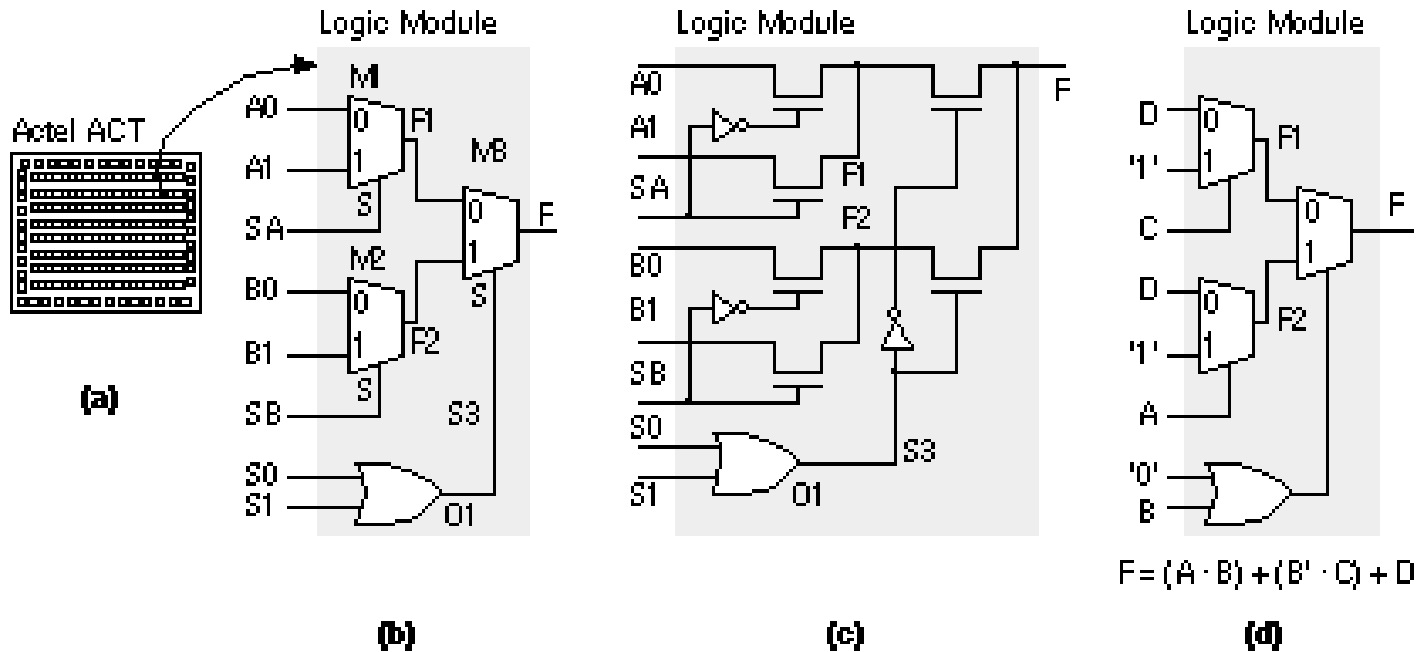
Actel ACT Logic Module

Multiplexer Logic as Function Generators

❑ Shannon's Expansion Theorem
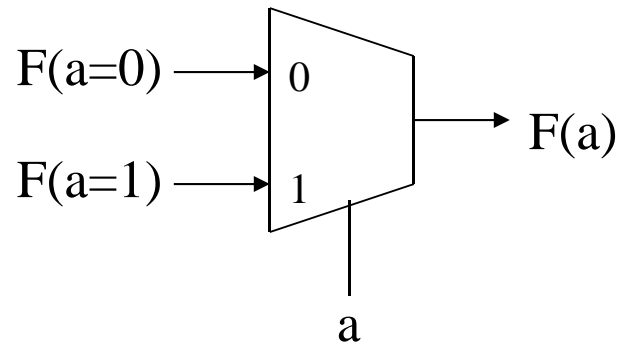
$$F(a) = a \bullet F(a{=}1) + a' \bullet F(a{=}0)$$

— $F(a{=}1)$ represents the function evaluated with $a{=}1$
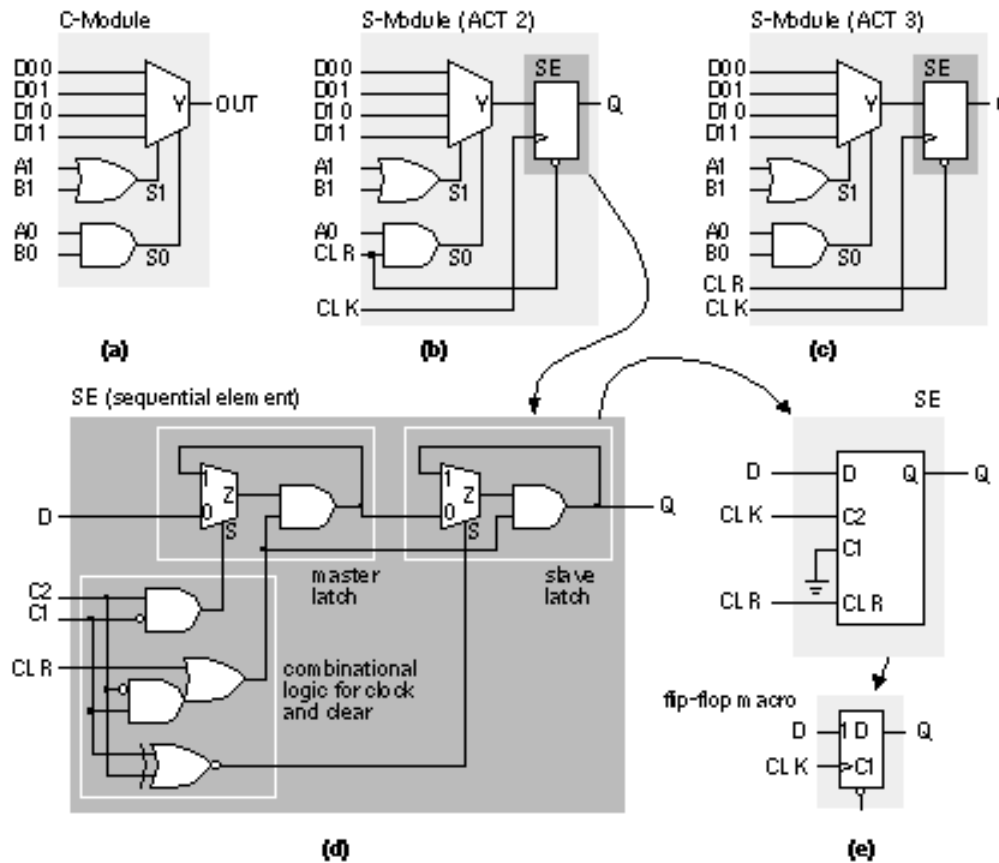— $F(a{=}0)$ represents the function evaluated with $a{=}0$

➤ example

$$F(a) = (b \bullet (a{+}c) + d \bullet a')'$$
$$= a \bullet b + a' \bullet (b \bullet c{+}d)'$$

❑ Implement F(a) using multiplexers

Actel ACT2 and ACT3 Logic Modules

❑ Flip-flop can be incorporated into a multiplexer-based logic module to implement sequential logic.

Memory Based Logic Cells

❑ A memory based logic cell is also called look-up table (LUT) based logic cell (memory is the LUT).

❑ Any function of up to K variables can be implemented by a k-input LUT (memory).

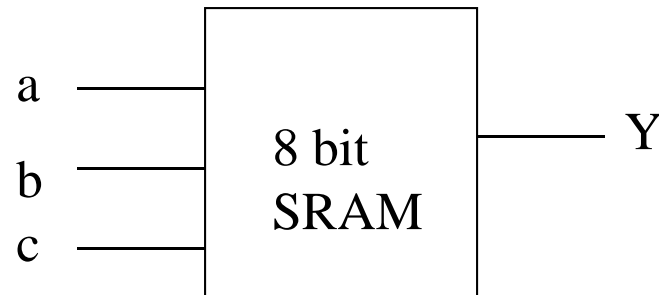❑ D flip-flops can be included in LUT based logic cells to implement sequential circuits.
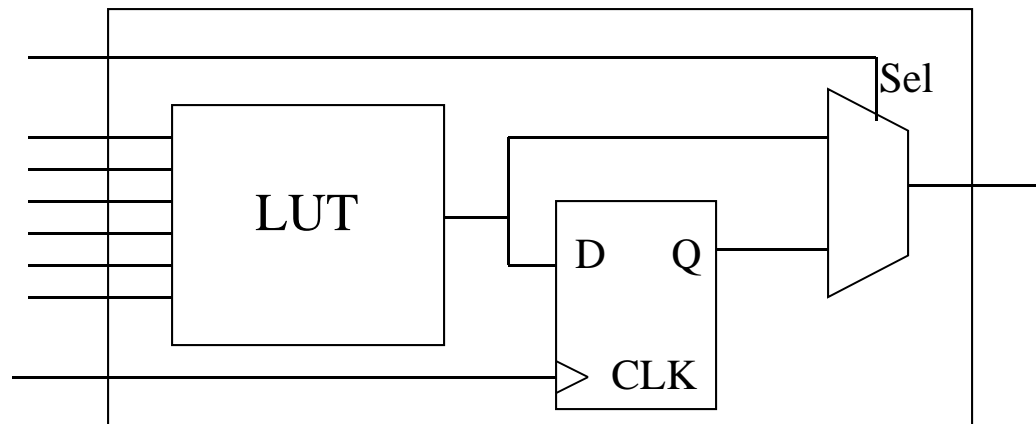
LUT-Based Logic Cell
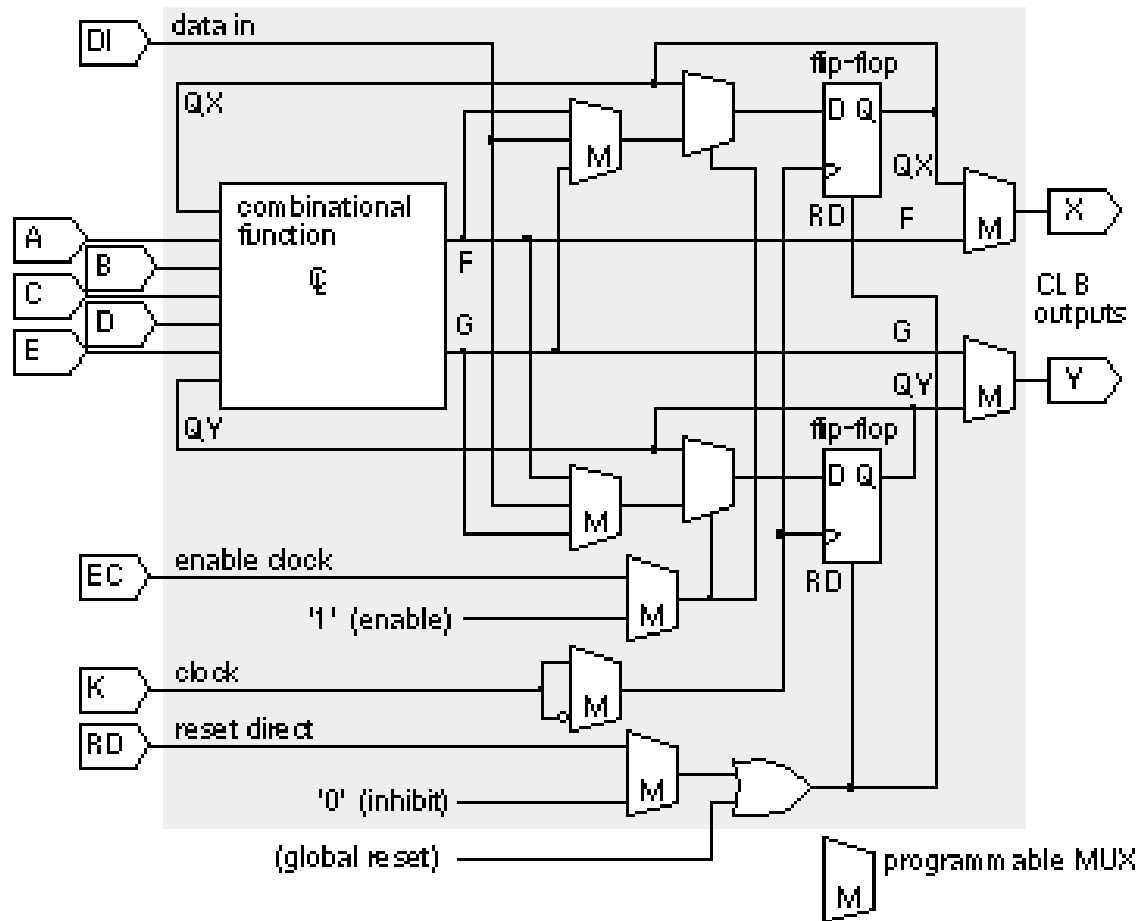
Function Implementation using LUT

❑ Implement Function $Y = a \cdot b + b \cdot c'$

a	b	c	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

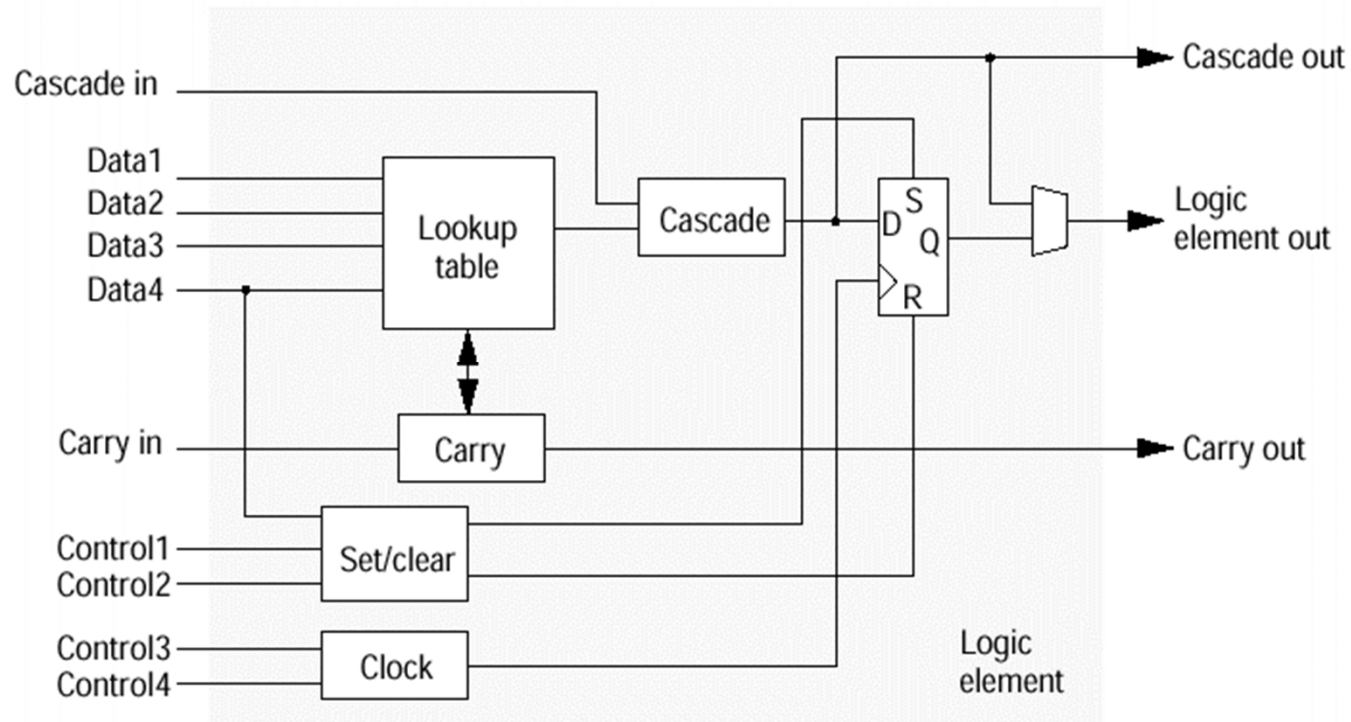Truth Table

a ——————
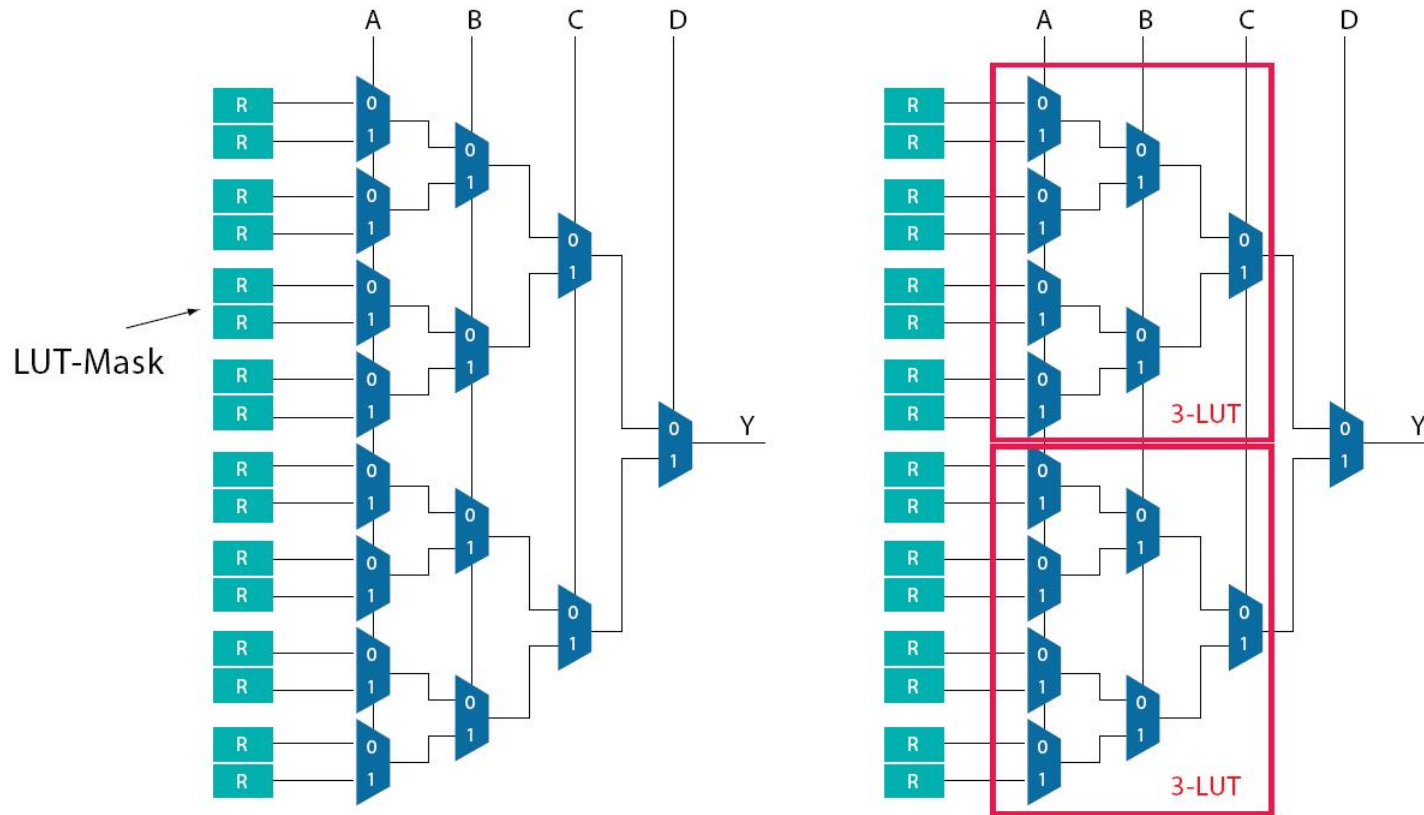b —————— 8 bit SRAM —————— Y
c ——————

Xilinx XC3000 Configurable Logic Block

Altera FLEX Logic Element

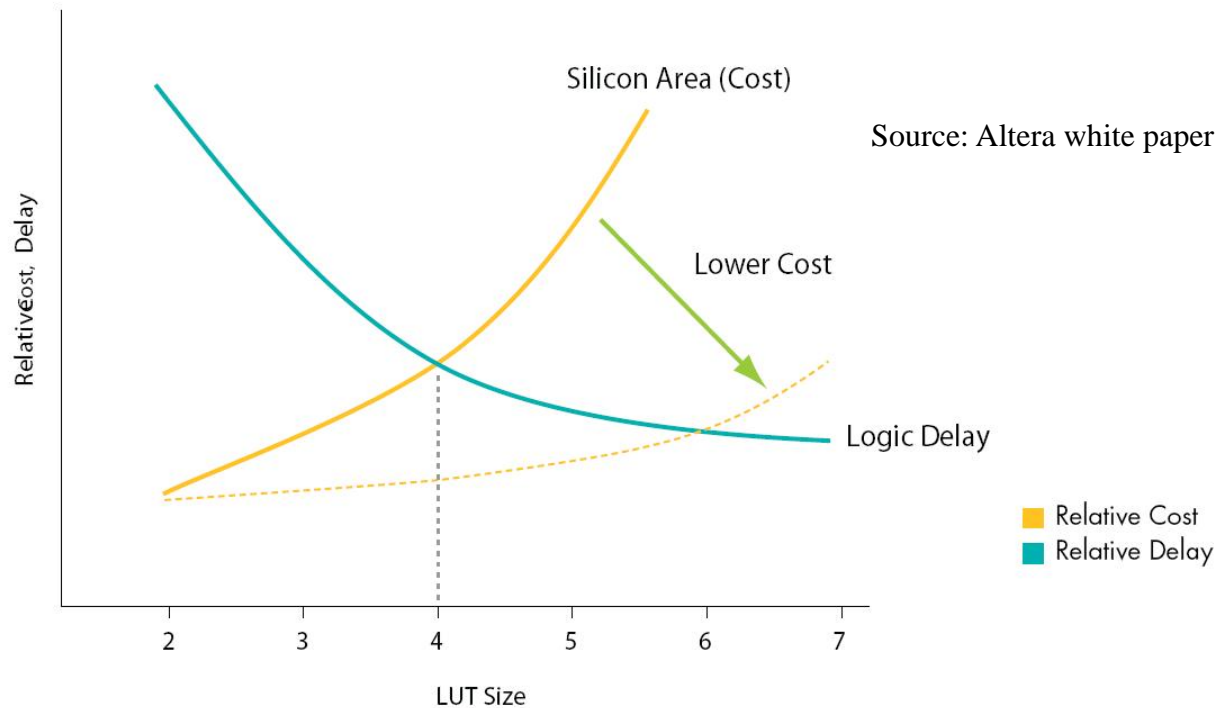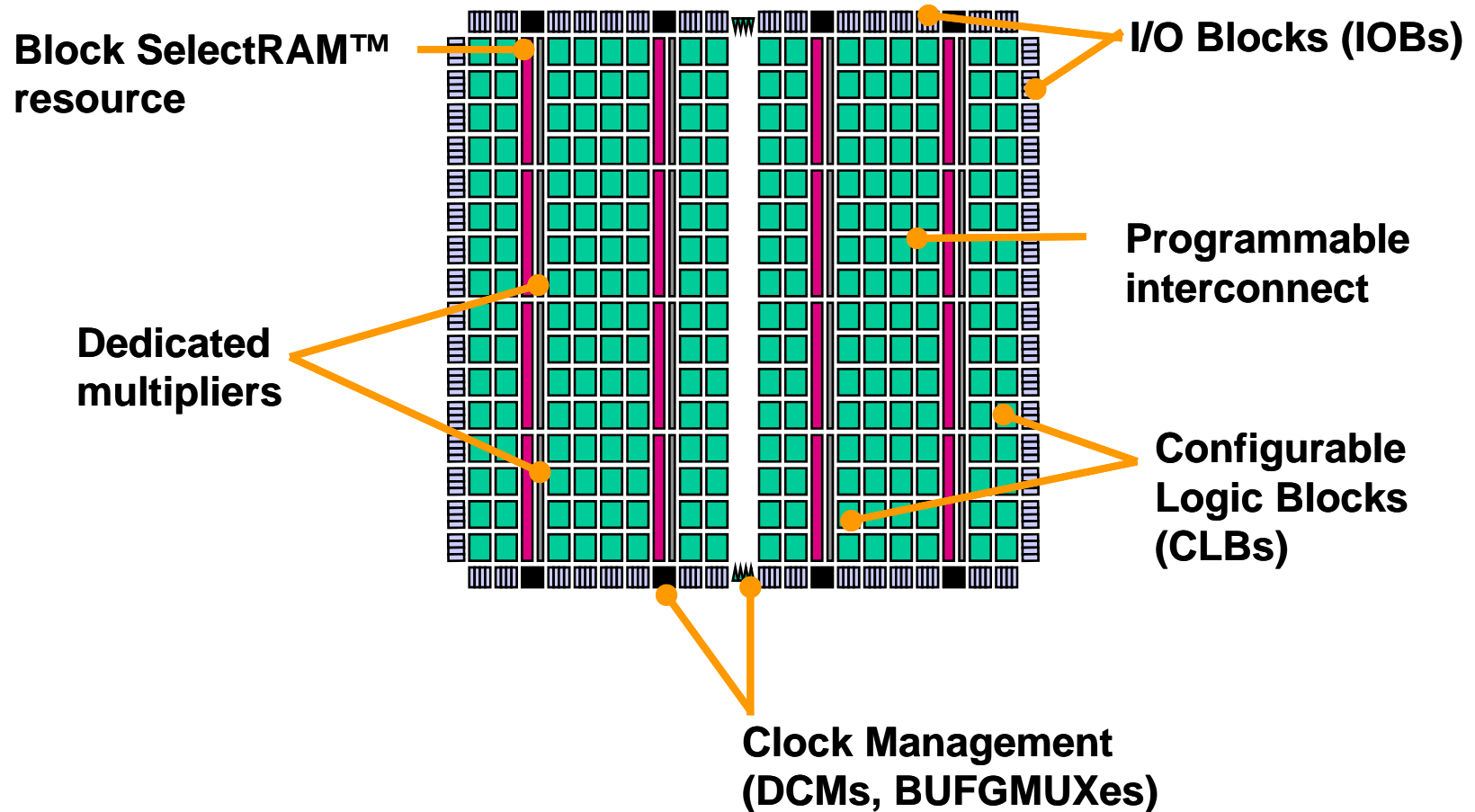# How to Build a LUT

Source: Altera white paper: FPGA Architecture

Determining the Optimal Size of LUT

Delay-Cost Tradeoff with LUT Size

Source: Altera white paper: FPGA Architecture
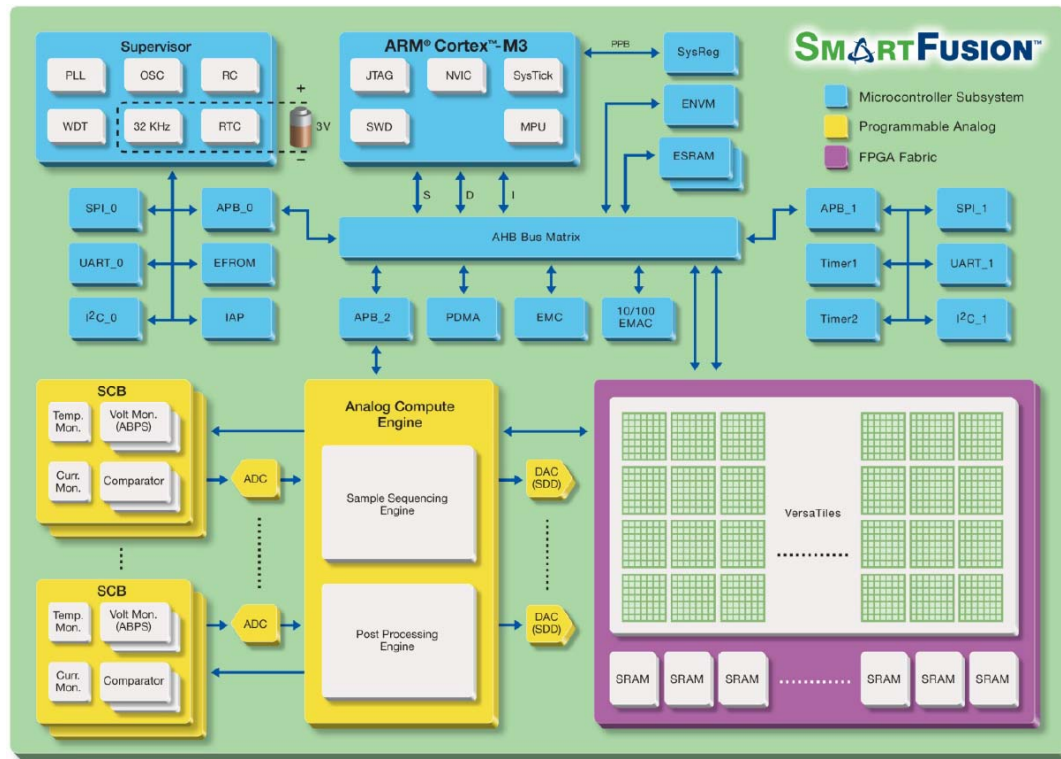
❑   Small size LUT increases the level of logic implementation
and, hence, increases circuit delay.
❑ Large size LUT increases silicon area and cost since some
of their inputs are not used in logic implementation.

Example: Xilinx Virtex II

Block SelectRAM™ resource

I/O Blocks (IOBs)

Dedicated multipliers

Programmable interconnect

Configurable Logic Blocks (CLBs)

Clock Management (DCMs, BUFGMUXes)

Source: Xilinx Basic FPGA Architecture

Adding Analog Flavor to Programmable Devices

❑ Some latest FPGA devices also contain programmable analog components to provide single-chip solutions for mixed-signal applications:

❑ Example: Actel SmartFusion

Source: www.actel.com