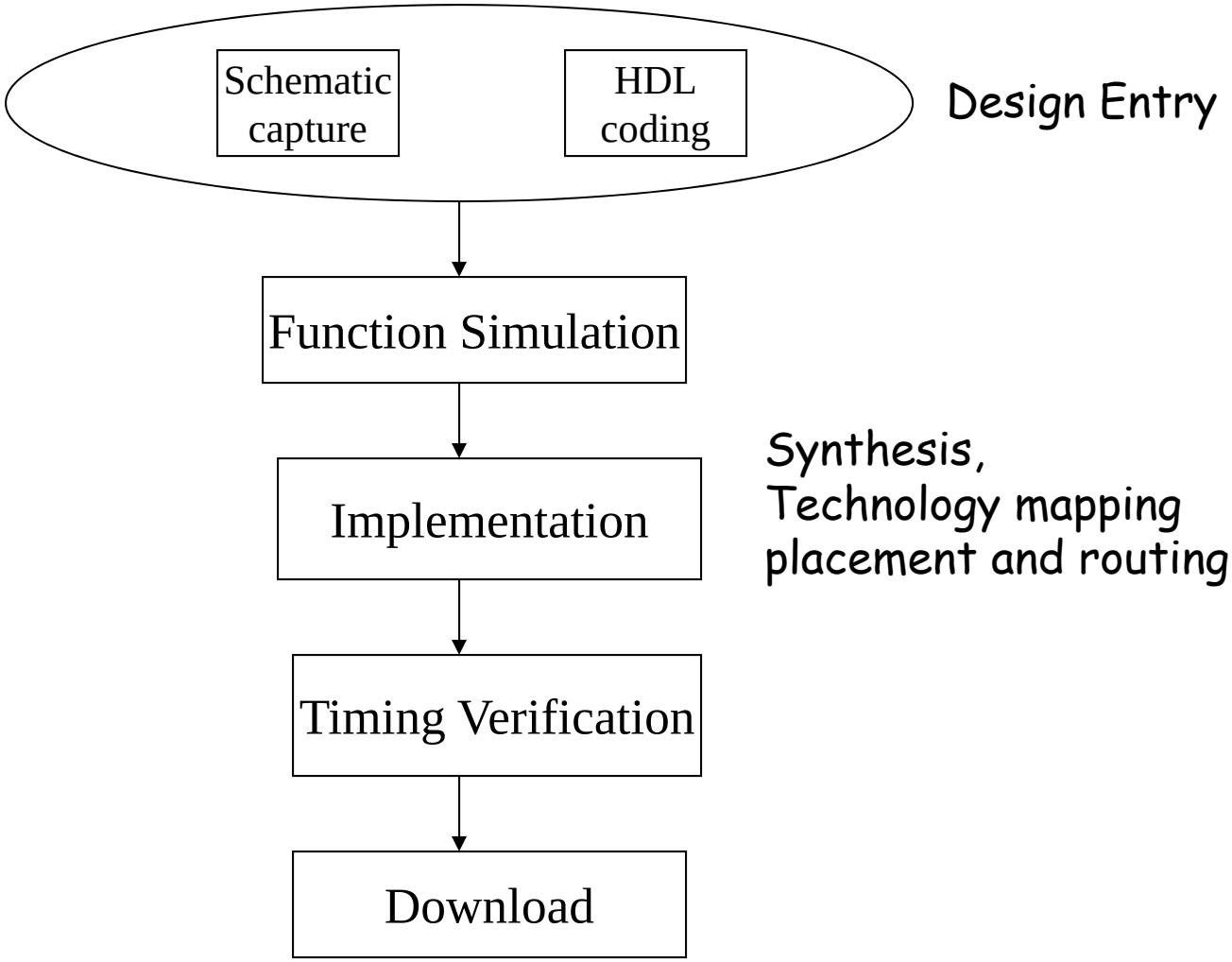
Timing Issues in FPGA Synchronous Circuit Design

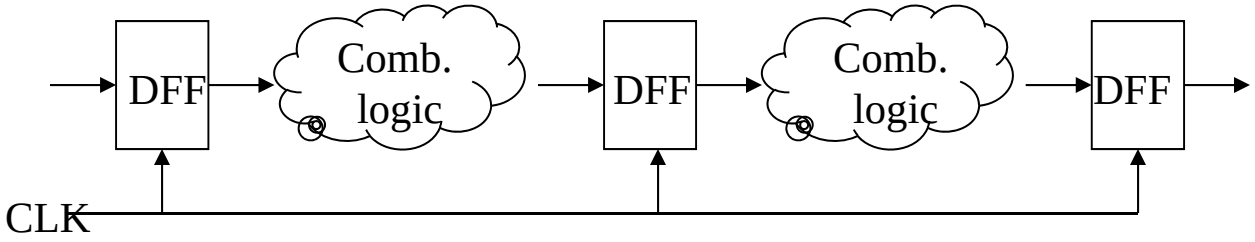
Haibo Wang
ECE Department
Southern Illinois University
Carbondale, IL 62901

FPGA Design Flow



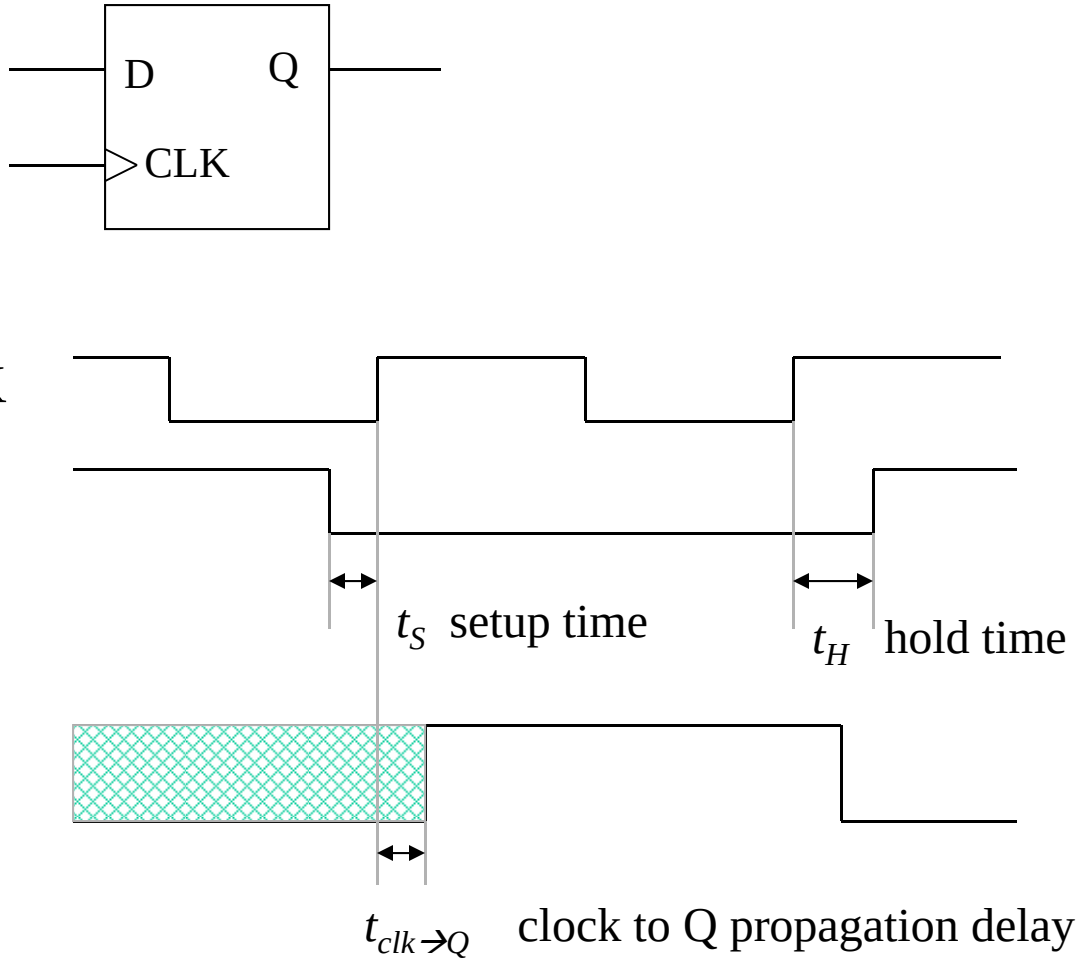
Introduction to Synchronous Circuits

- What are synchronous circuits?
  - In synchronous circuits, latching data in to memory elements (D flip-flops) are synchronized by a number of clocks.

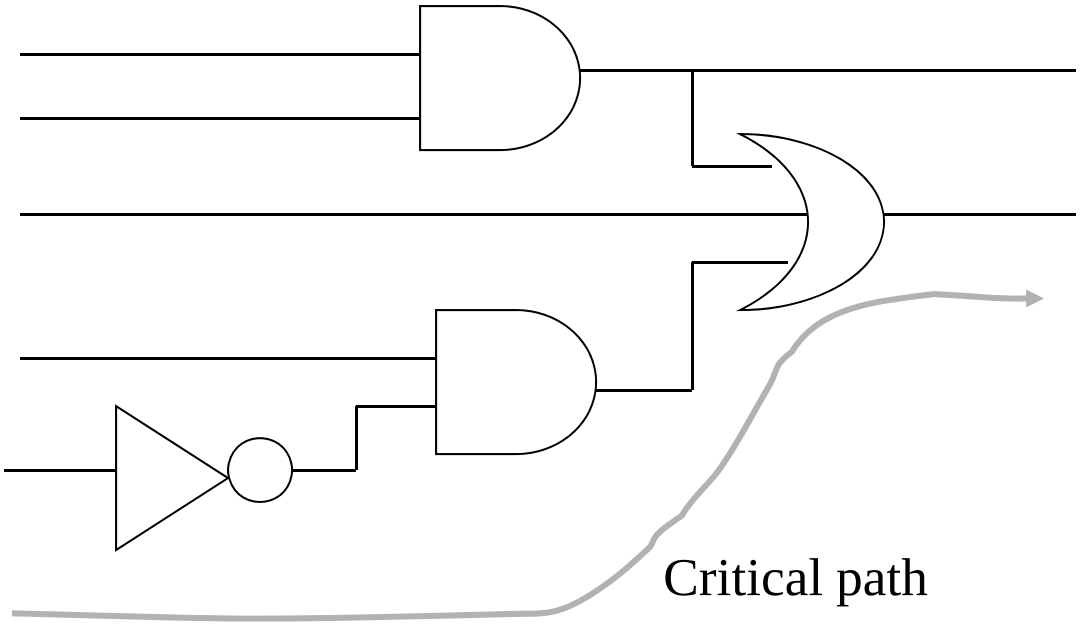


- Why synchronous design?
  - Well developed design methodologies
  - Easy to design, debug, and testing
  - Currently, most ASICs are synchronous circuits

D Flip-Flop Timing Parameters

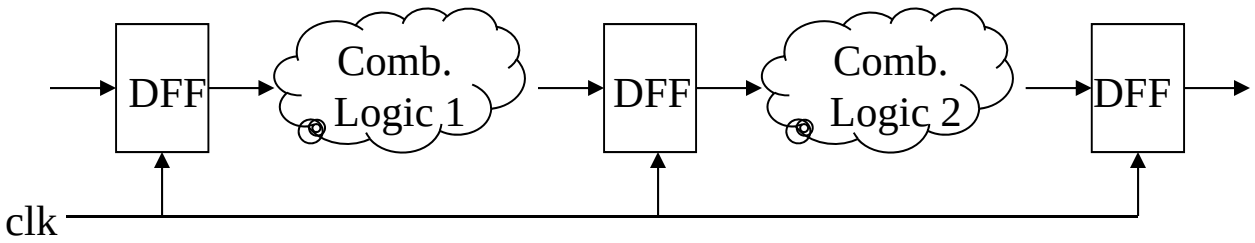


Critical Path in Combinational Circuits



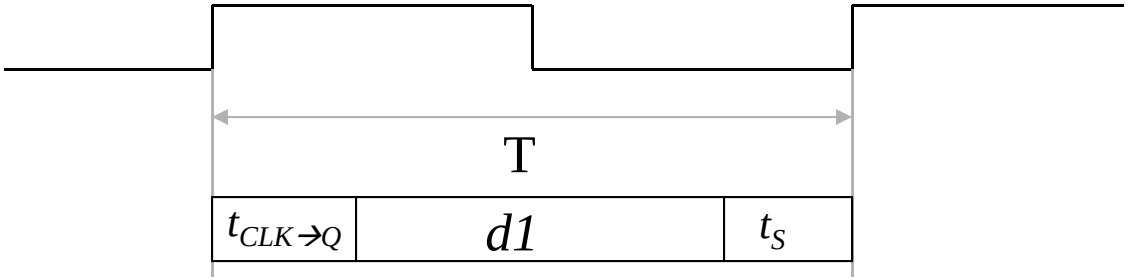
- **Critical Path:** The signal path that has the longest propagation delay
  - Assume that each gate has the same delay *d*
  - The delay of the critical path in the above circuit is 3•*d*

Determine Maximum Clock Frequency



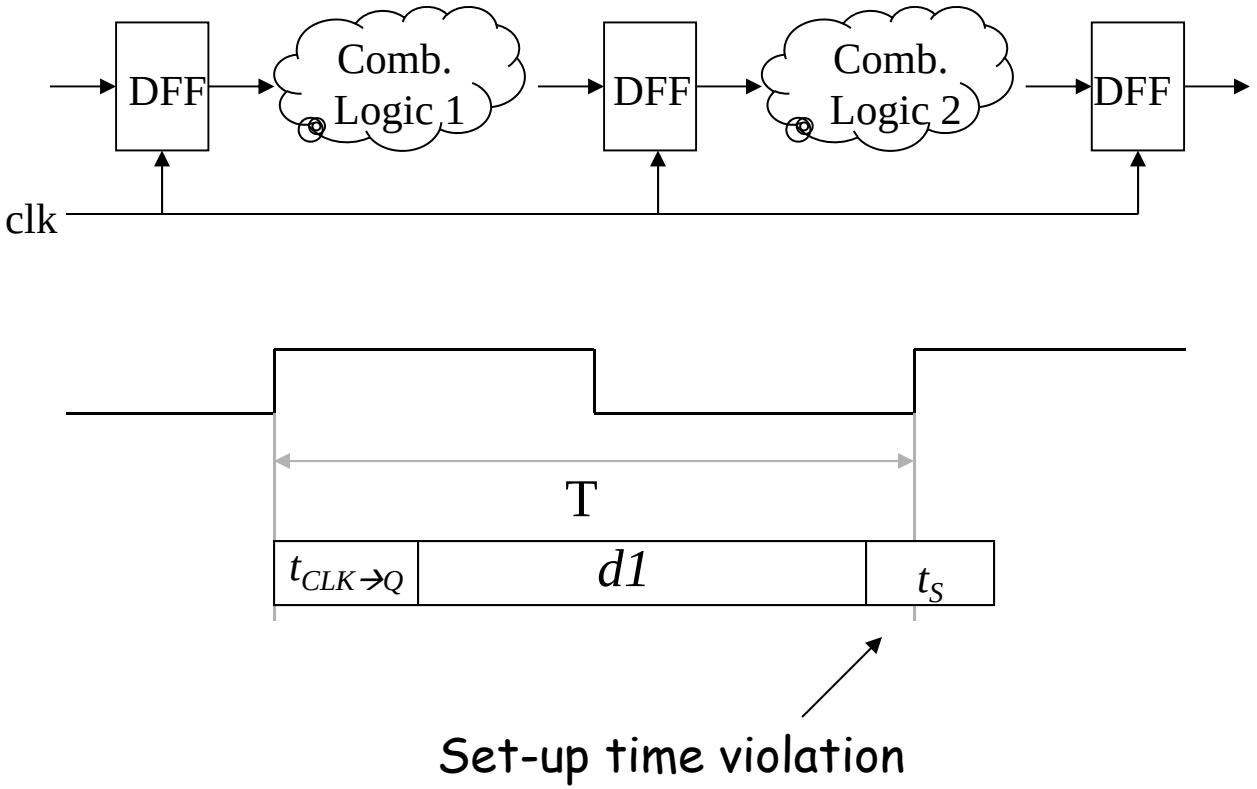
- The delays of the critical paths in comb. logic 1 and comb. Logic 2 are *d1* and *d2*, respectively. In addition, *d1>d2*

Minimum clock period T = $t_{CLK \rightarrow Q} + d1 + t_S$



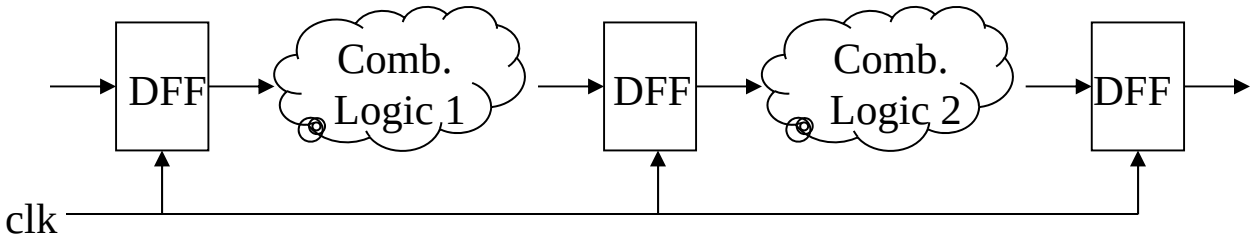
Slow Combinational Logic

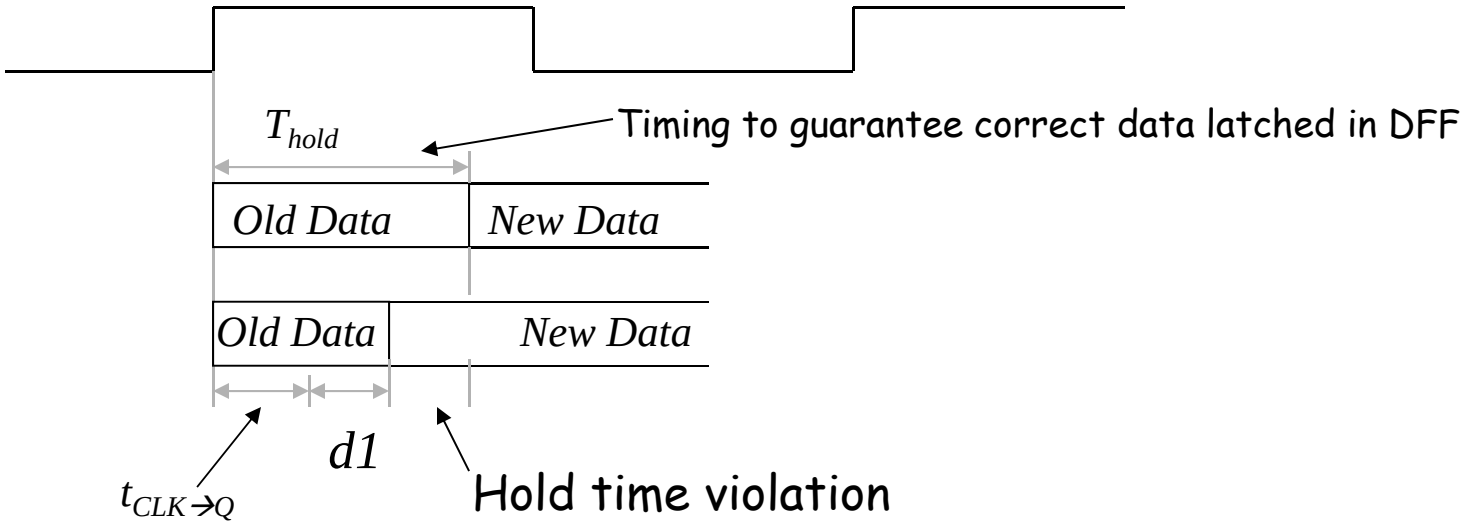
- Clock period is selected. The propagation delay of Comb. Logic 2 is too large



Too Fast Combinational Logic

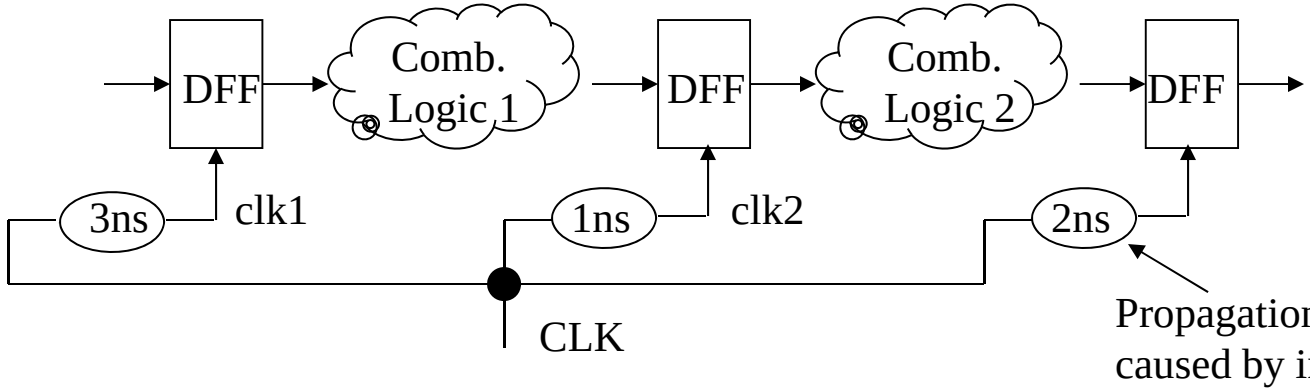
- Clock period is selected. The propagation delay of Comb. Logic 2 is too small

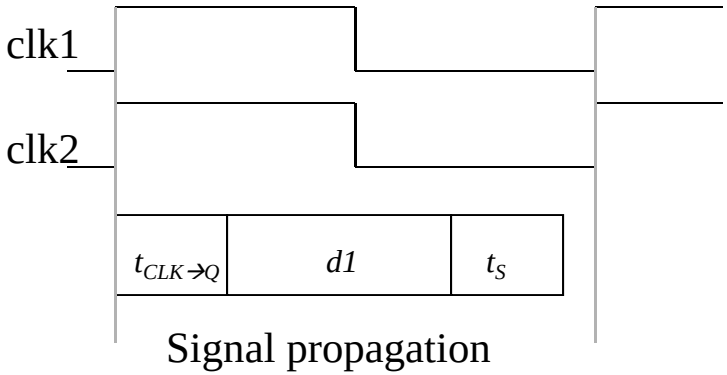




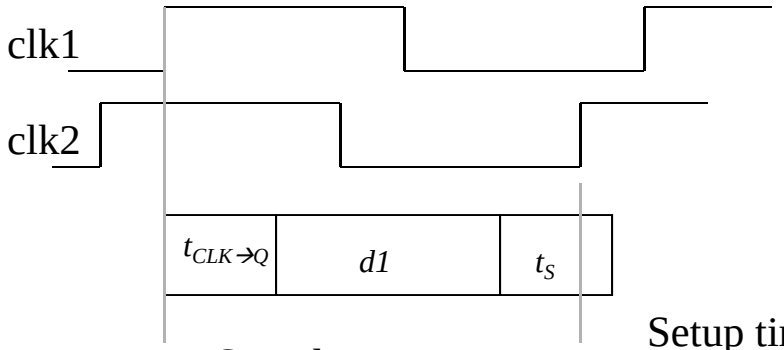
Clock Skew

- Due to interconnect delay, the same clock signal may switch at different time depending on the distance from the clock source. This effect is called clock skew.



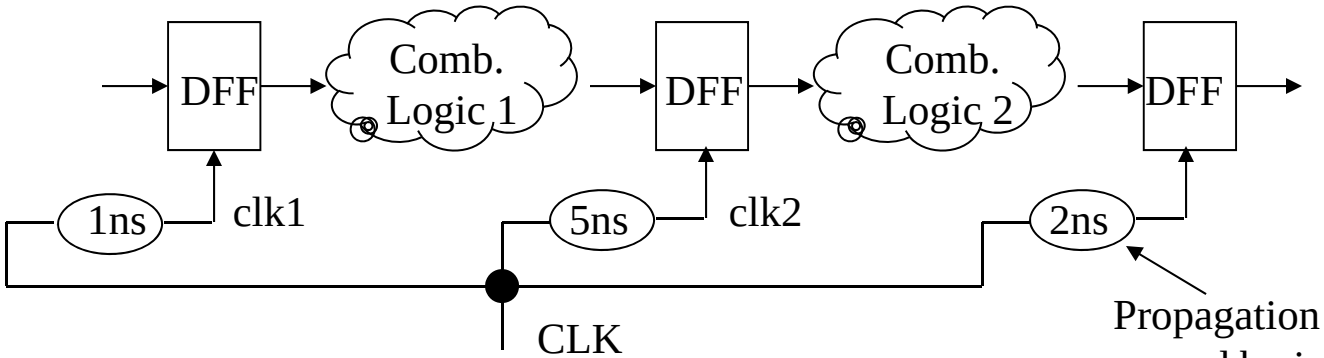


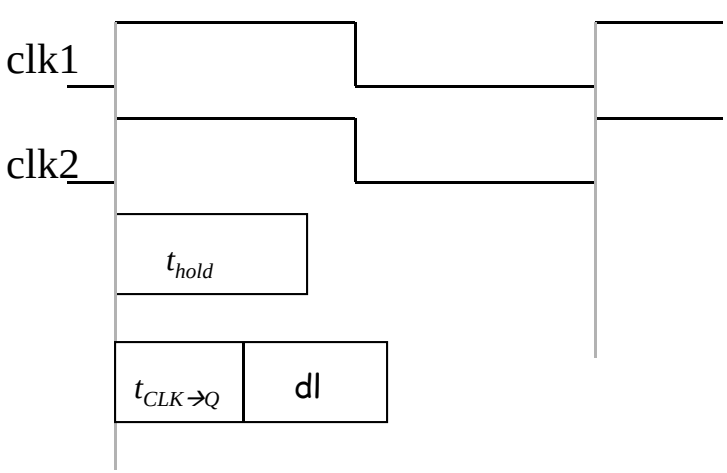
Without clock skew



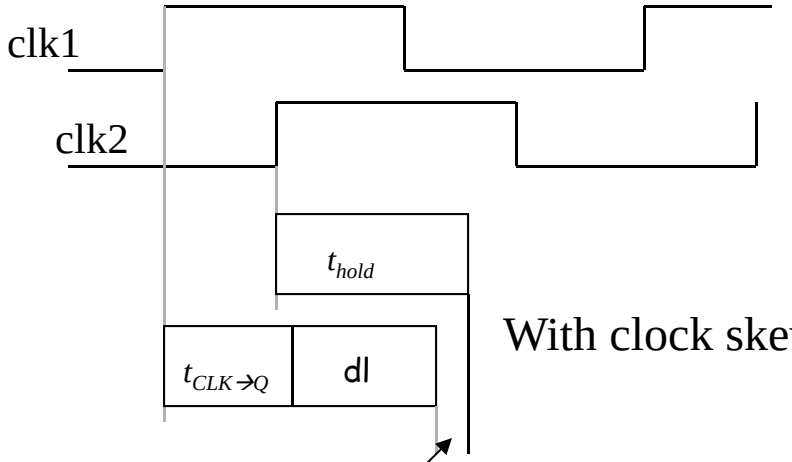
With clock skew

Clock Skew





Without clock skew



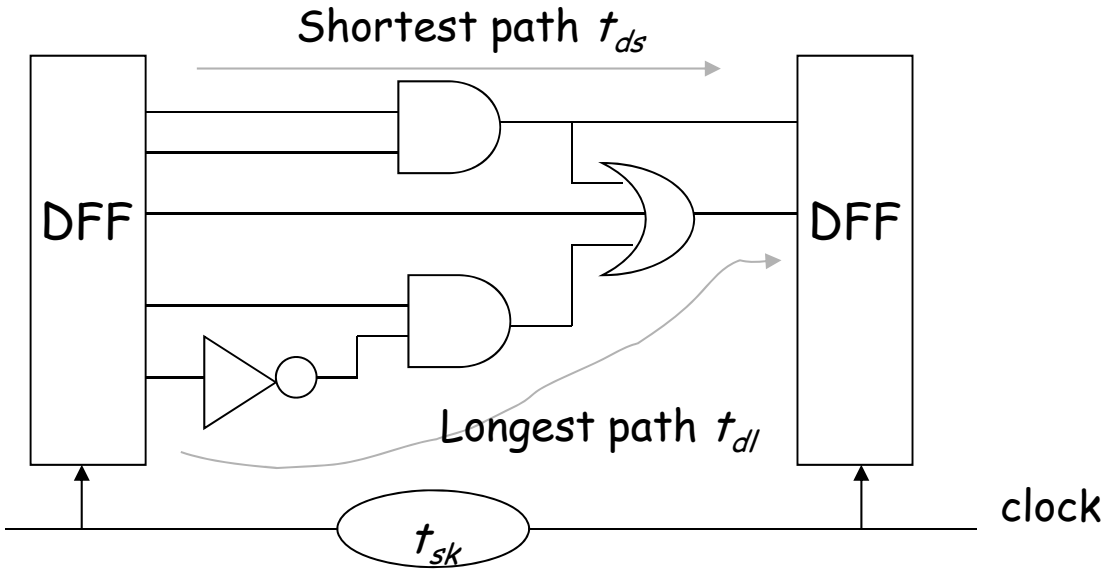
With clock skew

Hold time violation

Techniques to Reduce Clock Skew

- Use global buffers to distribute clock signals to minimize clock skew.
  - Modern FPGAs normally contain dedicated buffers (global buffers) to distribute clock signals around FPGA chips.
  - The global buffers are connected through specially balanced routing resources to minimize clock skew.
  - Use symbol BUFG to indicate the use of global buffers in schematic entry. Most synthesis tools can automatically use global buffers for clock signals
  - In latest FPGAs, more sophisticated circuit techniques, such as Phase-Locked Loop (PLL), are used to minimize clock skew .

Timing Constraints in Synchronous Circuits



- To avoid setup time violation

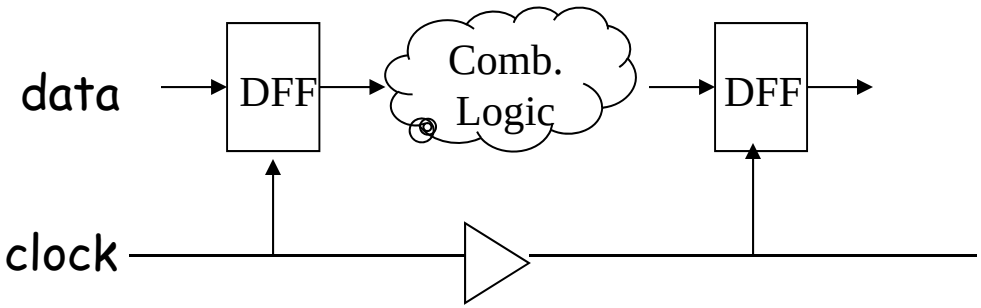
$$t_{clk->Q} + t_{dl} + t_{setup} \leq T_{clk} + t_{sk}$$

- To avoid hold time violation

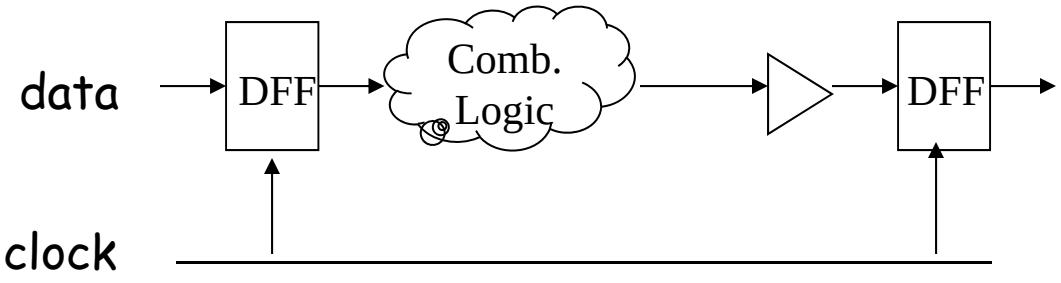
$$t_{clk->Q} + t_{ds} \geq t_{hold} + t_{sk}$$

Techniques to Avoid Timing Violations

- Insert delay elements on clock path to avoid setup time violations

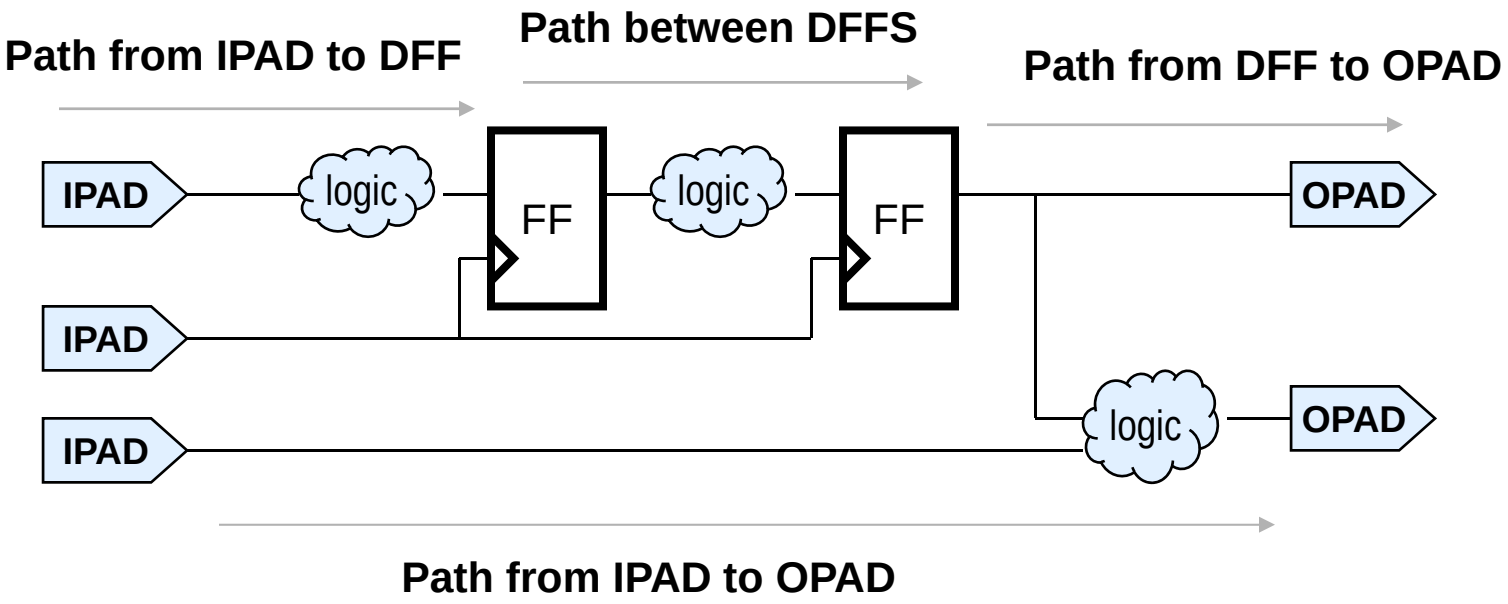


- Insert delay elements on data path to avoid hold time violations



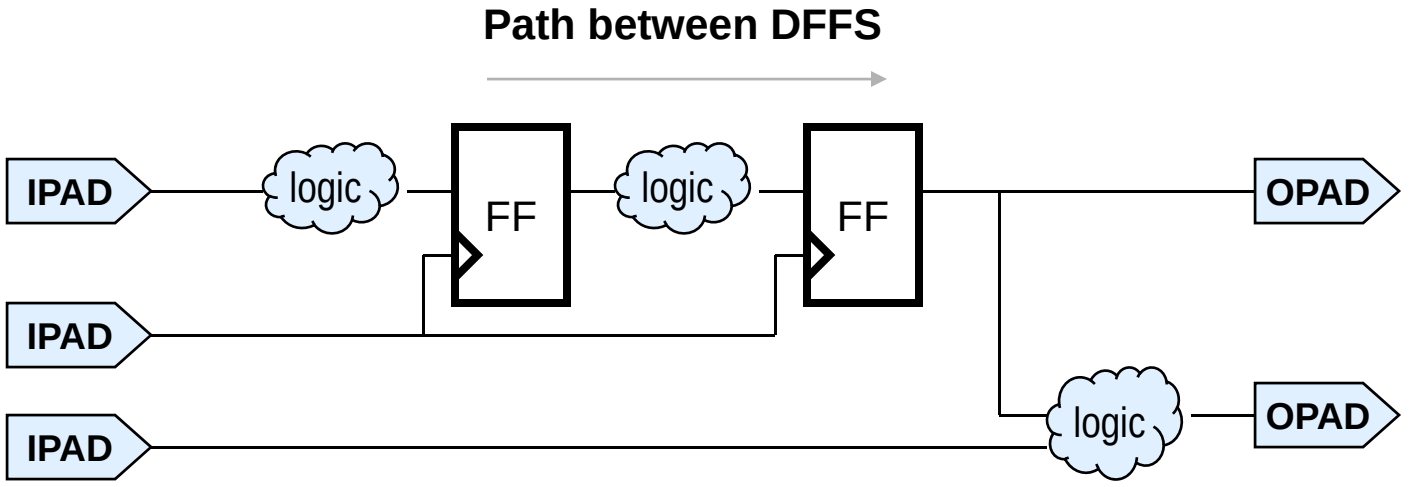
Specifying Timing Constraints in ASIC Design

- Timing constraints are used to specify delay of circuit paths
- The end points of paths can be D flip-flops, Latches, Input or Output pads, and Memories



Period Constraint

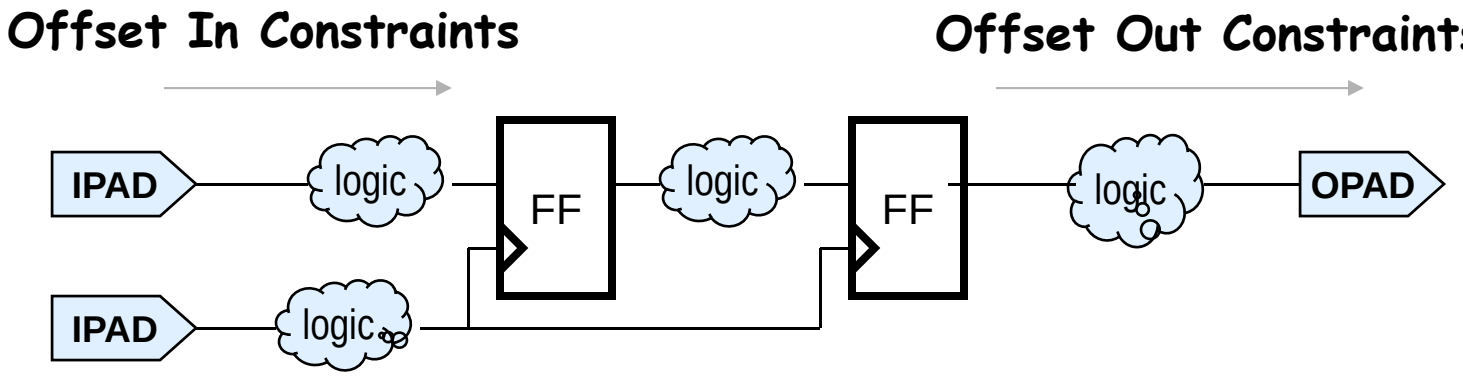
- Period constraints specify delay of paths between synchronous elements that are clocked by the same clock
  - Period constraint is also called register-to-register delay
  - Synchronous elements include D flip-flops, latches, and synchronous Rams
  - In the following example, the period constraint specify delay of a path between two D flip-flops



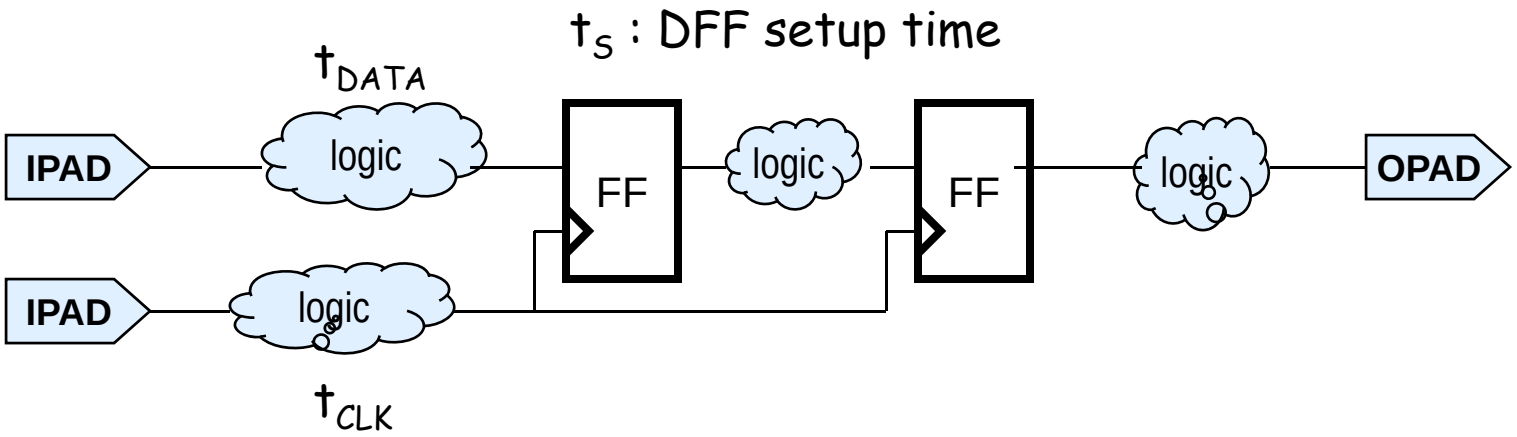
The delay of the path $t_{dl} < T - t_{CLK \rightarrow Q} - t_S$

Offset Constraint

- Offset constraints specify delays of paths:
  - From input pads to synchronous elements. The constraints for this type paths are called as offset in constraints. For the input paths, external setup time and external hold time have to be considered
  - From synchronous elements to output pads. The constraints for this type paths are called as offset out constraints.



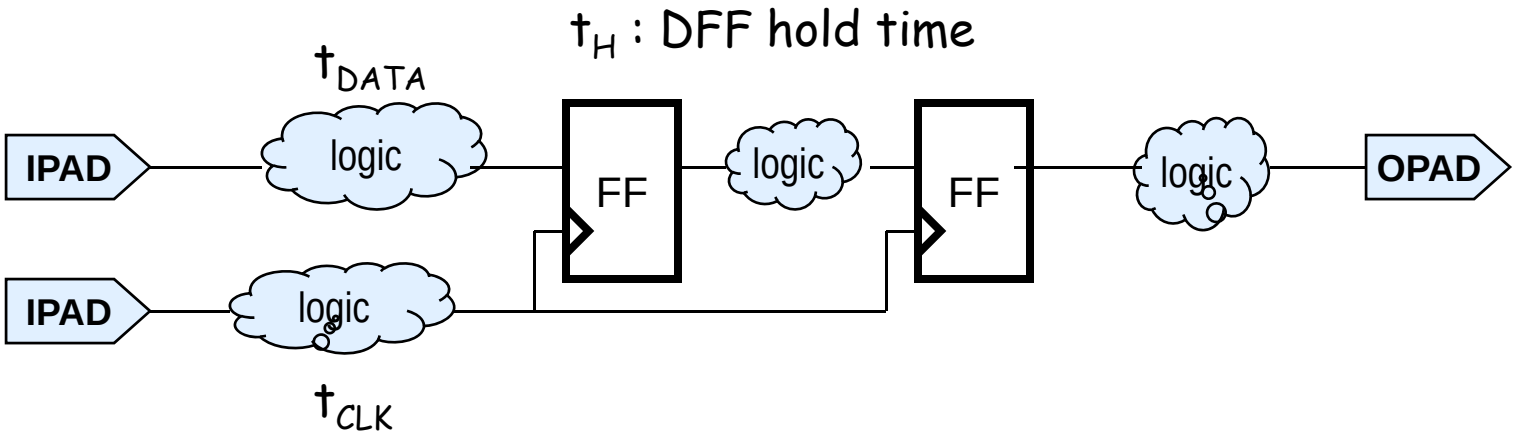
External Setup Time



- Worst case setup time for input occurs when input is DELAYED relative to CLK. Means clock edge arrives early, requiring input to be ready sooner.

External setup time = $t_S + t_{DATA}(max) - t_{CLK}(min)$

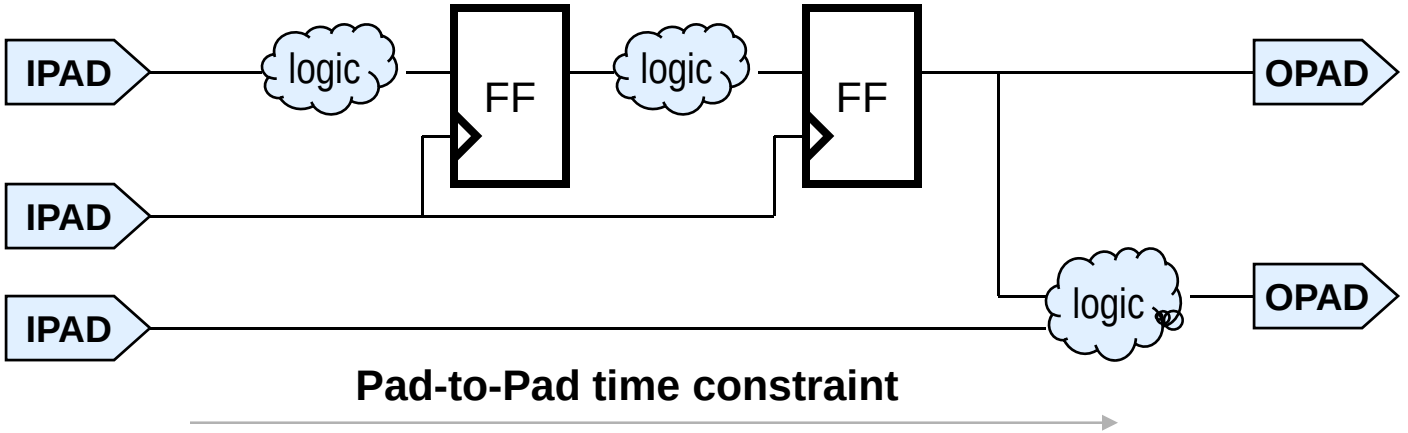
External Hold Time



- Worst case hold time for input occurs when CLK is DELAYED relative to input. Means clock edge arrives late, requiring input to hold its value longer.

External hold time = $t_H + t_{CLK}(max) - t_{DATA}(min)$

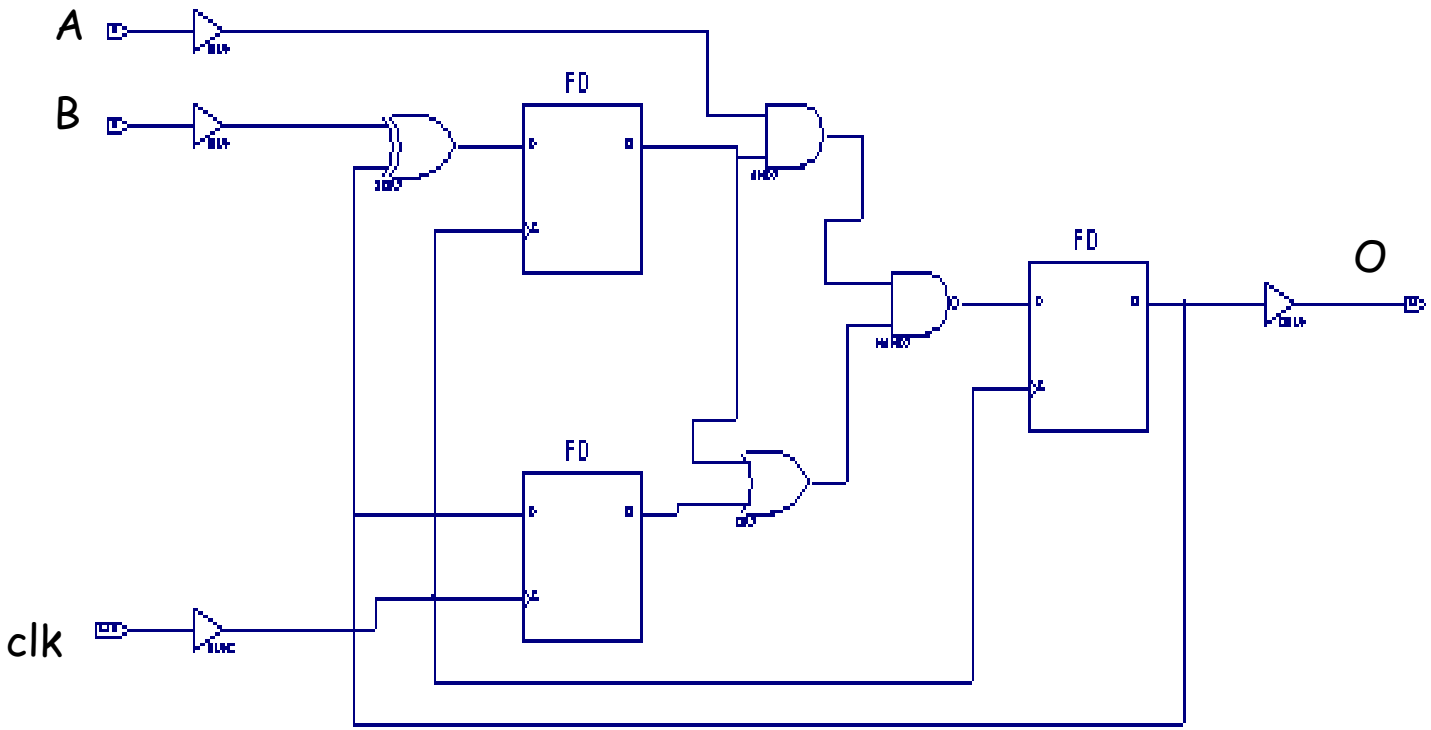
Pad-to-Pad Time Constraint



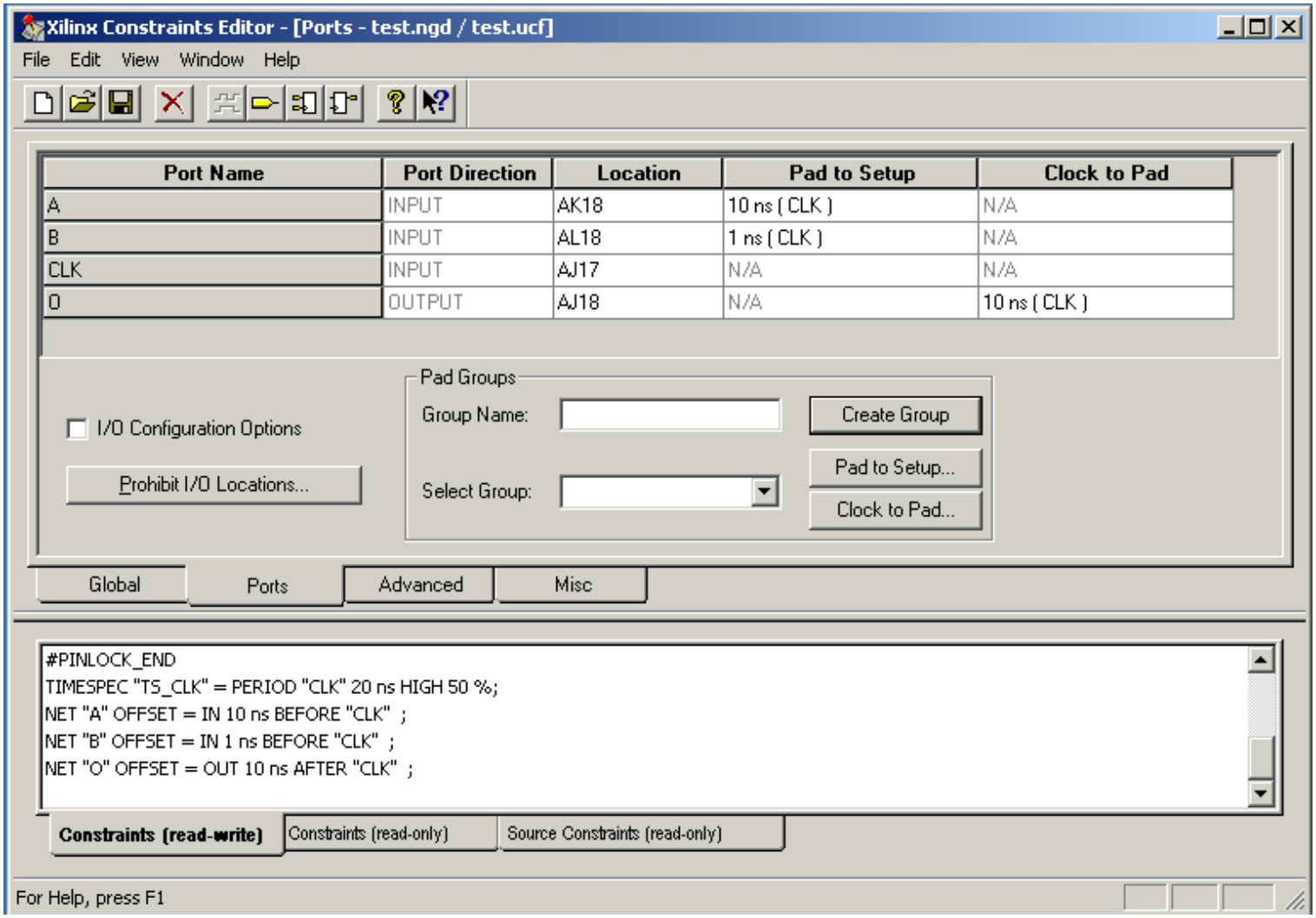
- It specifies delays for paths that are from input pads to output pads
- Purely combinatorial delay paths do not contain any synchronous elements

Specifying Time Constraints in Xilinx Tools

- Example circuit



Specifying Time Constraints in Xilinx Tools

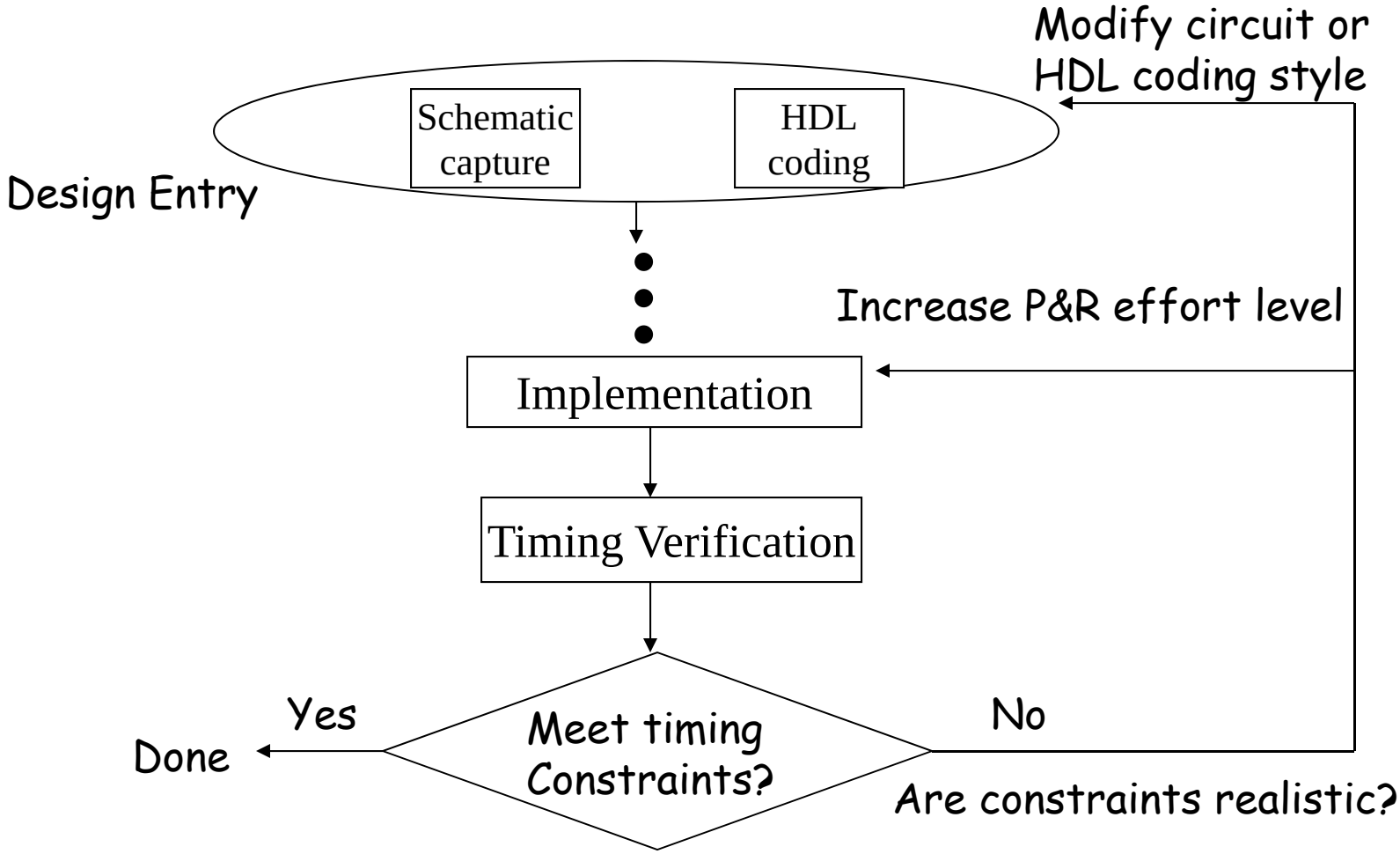


Report from Static Timing Analysis

Asterisk (*) preceding a constraint indicates it was not met.
This may be due to a setup or hold violation.

Constraint	Requested	Actual	Logic Levels
TS_CLK = PERIOD TIMEGRP "CLK" 20 nS HIGH 50.000000 %	20.000ns	3.568ns	1
COMP "A" OFFSET = IN 10 nS BEFORE COMP "CLK"	10.000ns	1.788ns	2
* COMP "B" OFFSET = IN 1000 pS BEFORE COMP "CLK"	1.000ns	1.334ns	2
COMP "O" OFFSET = OUT 10 nS AFTER COMP "CLK"	10.000ns	9.352ns	1

Flow for Achieving Timing Closure



What Affect Circuit Timing Performance

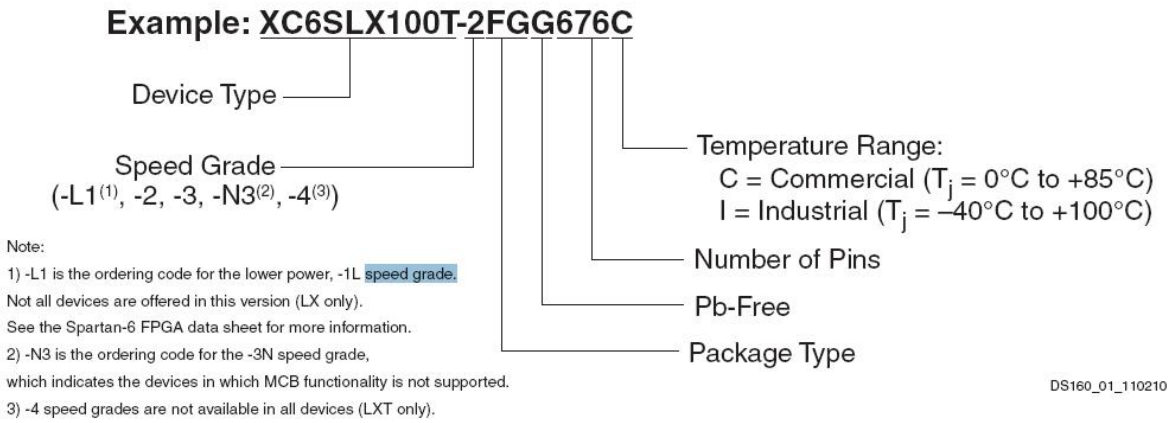
❖ Environmental factors

- ❑ Commercial Products are expected to work in the following environment
  - — Supply voltage varies 10%
  - — Temperature from 0 to 85 °C
- ❑ Fast Corner (circuits have small delay)
  - — Supply voltage: V_{DD} + V_{DD}•10%; Temperature: 0 °C
- ❑ Slow Corner (circuits have large delay)
  - — Supply voltage: V_{DD} - V_{DD}•10%; Temperature: 85 °C
- ❑ Perform timing analysis at fast corner to check hold time violations and perform timing analysis at slow corner to check setup time violations

What Else Affect Circuit Timing Performance

- Process variations
  - NFET (fast, slow, typical)
  - PFET (fast, slow, typical)
  - Interconnect (fast, slow, typical)

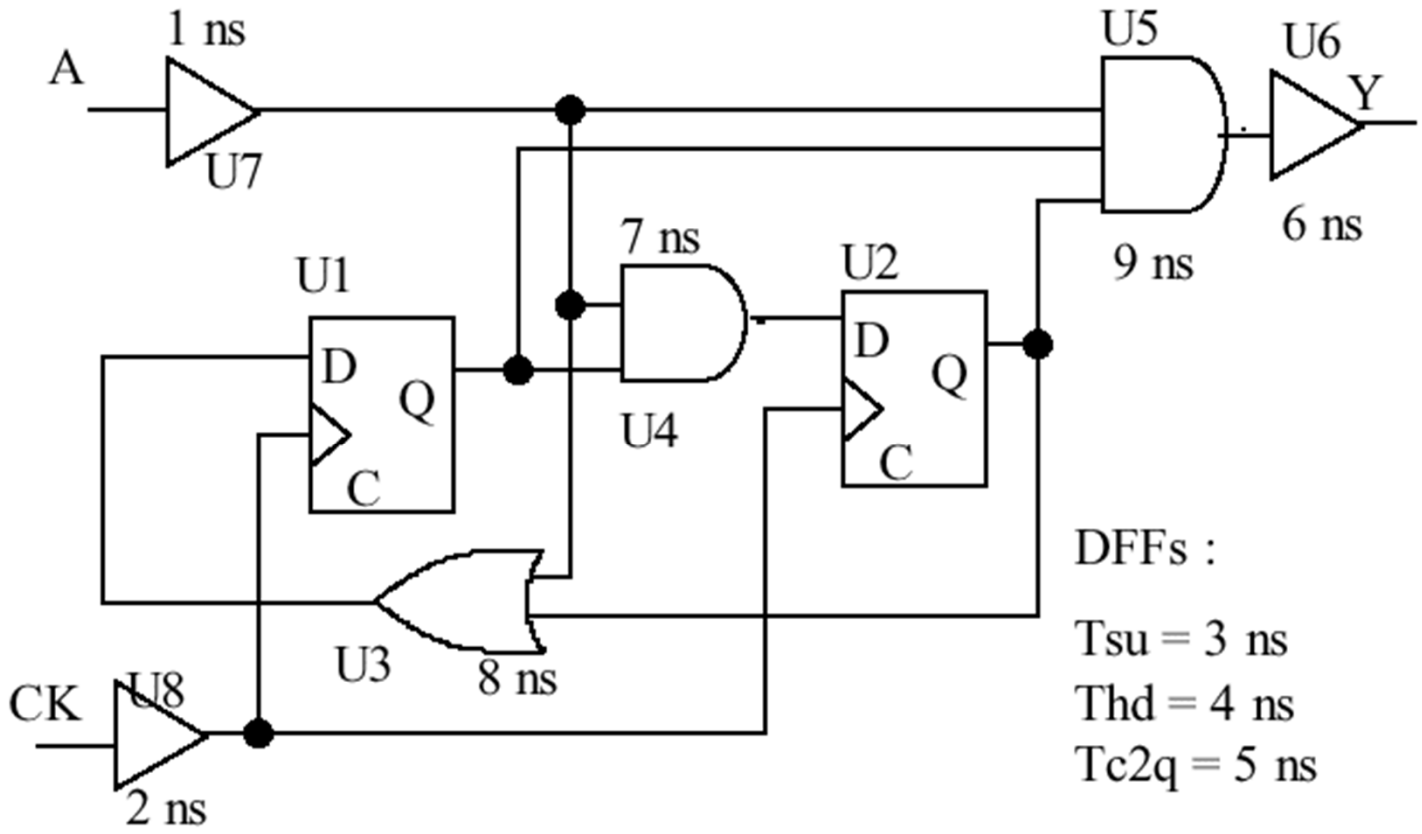
- Due to process variations and other factors, including operating voltage, circuit design, etc, devices from the same family can achieve different operating speeds:



Source: www.xilinx.com

Example on Calculating Timing Parameters

- Calculate timing parameters



Calculating Timing Parameters

- Maximum register to register delay

  U2 Tc2q + U3 Tpd + U1 Tsu= 5 + 8 + 3 = 16 ns.

- External setup time

  Tsu + A2D Tpd max - Clk Tpd min = 3 + (8 + 1) - 2 = 10 ns

- External hold time

  Thd + Clk Tpd max - A2D Tpd min = 4 + 2 - (7 + 1) = -2 ns

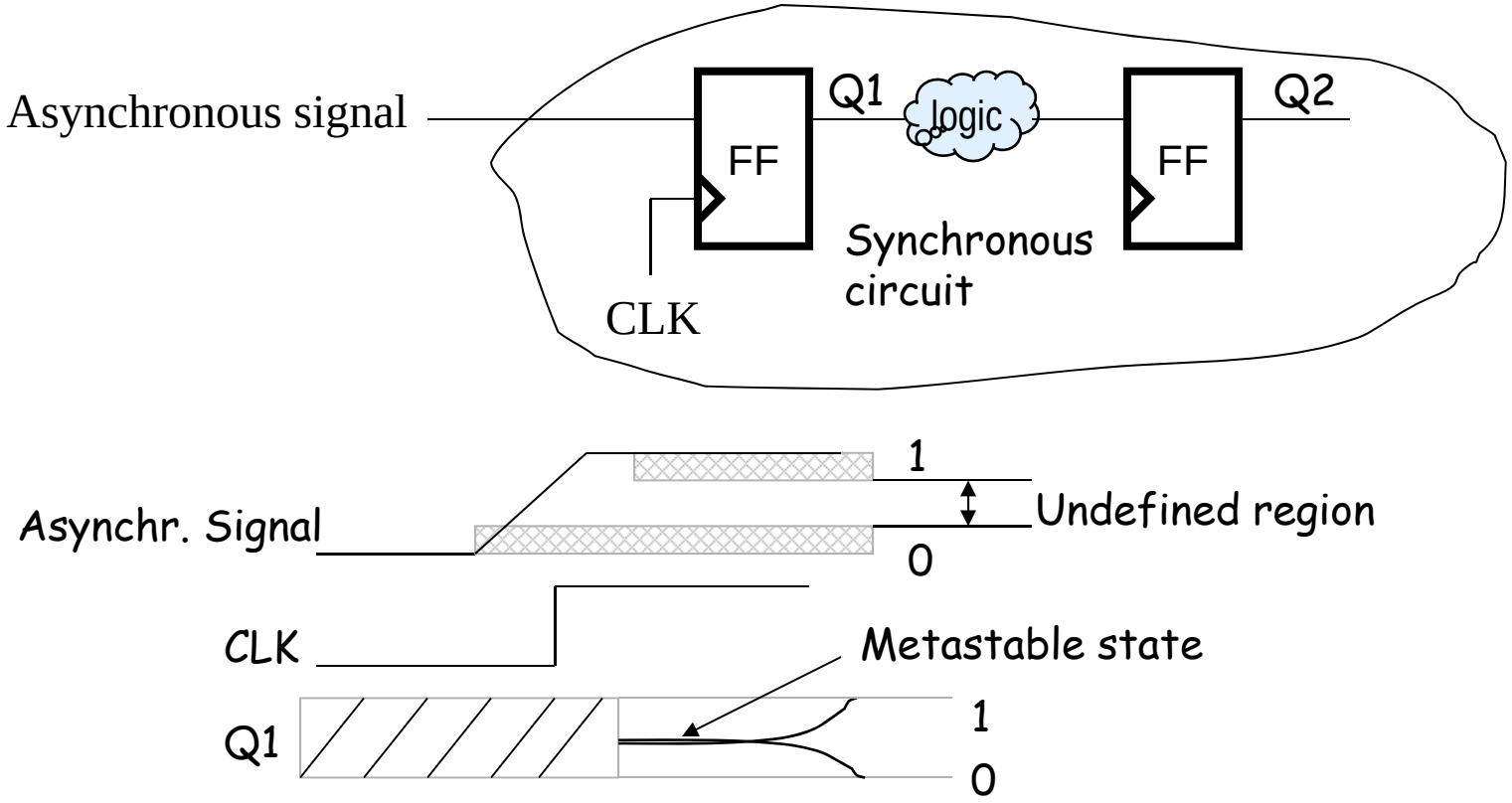
- Clock to Out Delay

  U8 Tpd + U2 Tc2q + U5 Tpd + U6 Tpd = 2 + 5 + 9 + 6 = 22 ns

- Pad to pad Delay

  U7 Tpd + U5 Tpd + U6 Tpd = = 1 + 9 + 6 = 16 ns

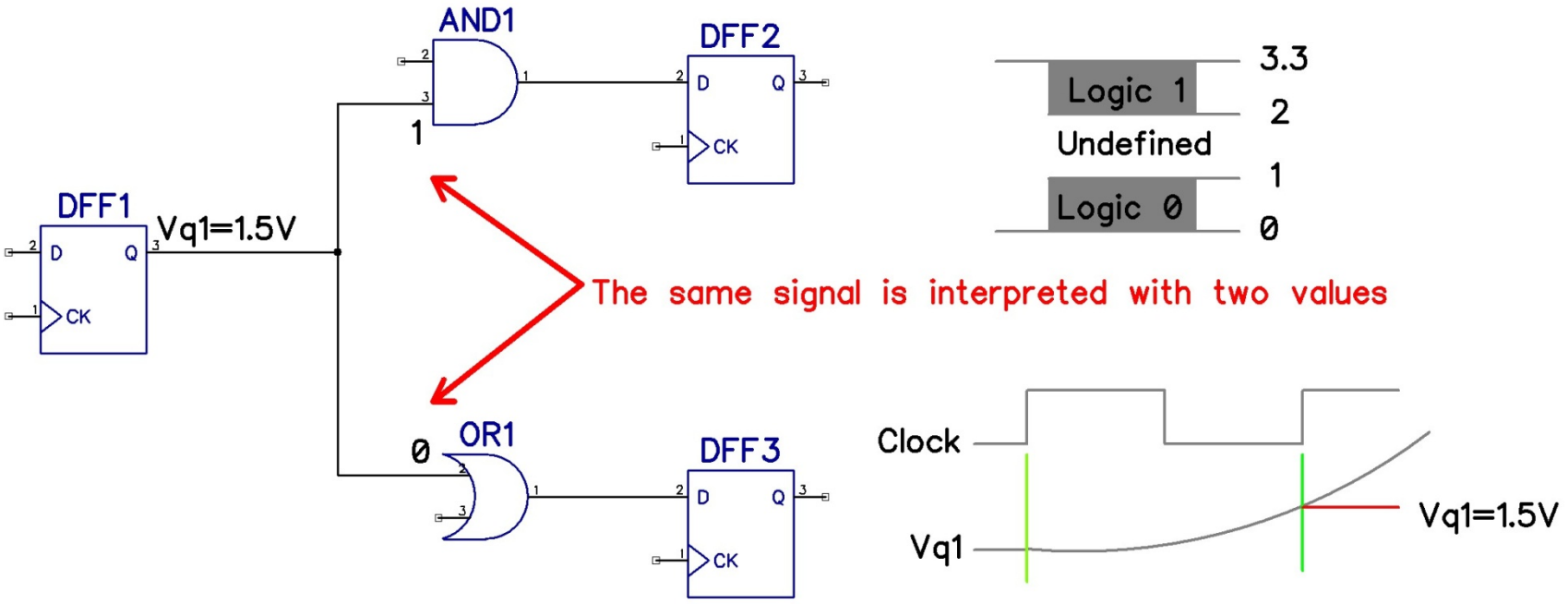
Interface with Asynchronous Inputs



- If the asynchr. input is in undefined region when the DFF latches it, the DFF output will be possibly in metastable state. The DFF output will eventually settle to logic 1 or 0. However, this process must complete with a certain period. Otherwise, it will be a failure.

Potential Problems of Metastability

❑ Due to metastability, the same signal may be treated as having different logic values in different part of the circuit



Metastability Analysis

- Mean Time Between Failure: MTBF

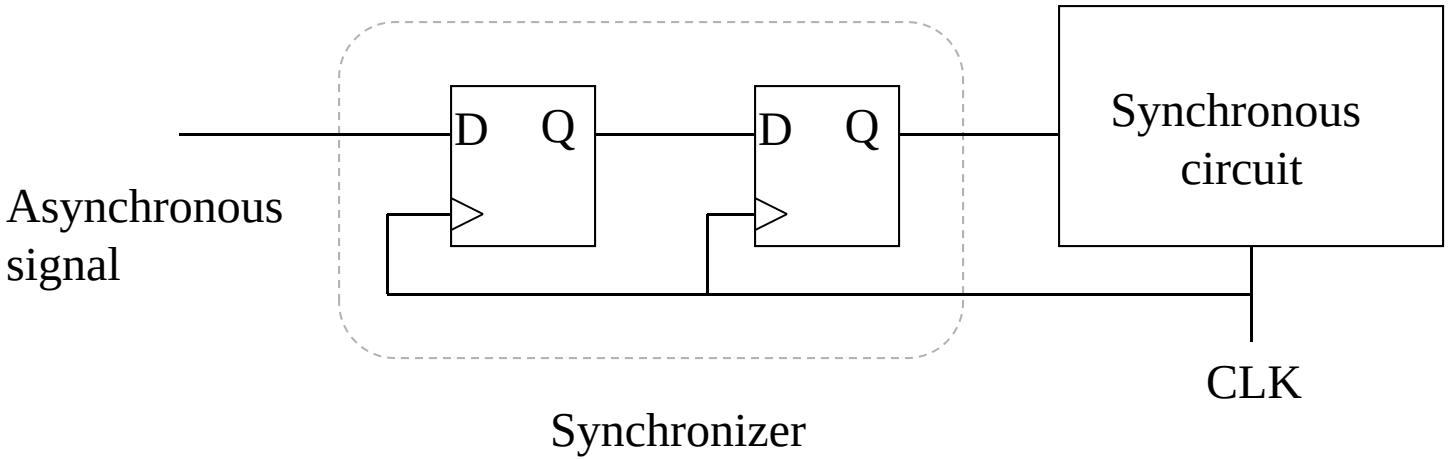
$$MTBF = \frac{e^{\frac{t_r}{\tau}}}{T_0 \bullet f_{in} \bullet f_{clock}}$$

Where,

1. t_r is metastability resolution time, maximum time the output can remain metastable without causing synchronizer failure.
2. T_0 and τ are constants that depend on the electrical characteristics of the flip-flop.
3. f_{in} is the frequency of the asynchronous input
4. f_{clock} is the frequency of the sampling clock

Increasing MTBF

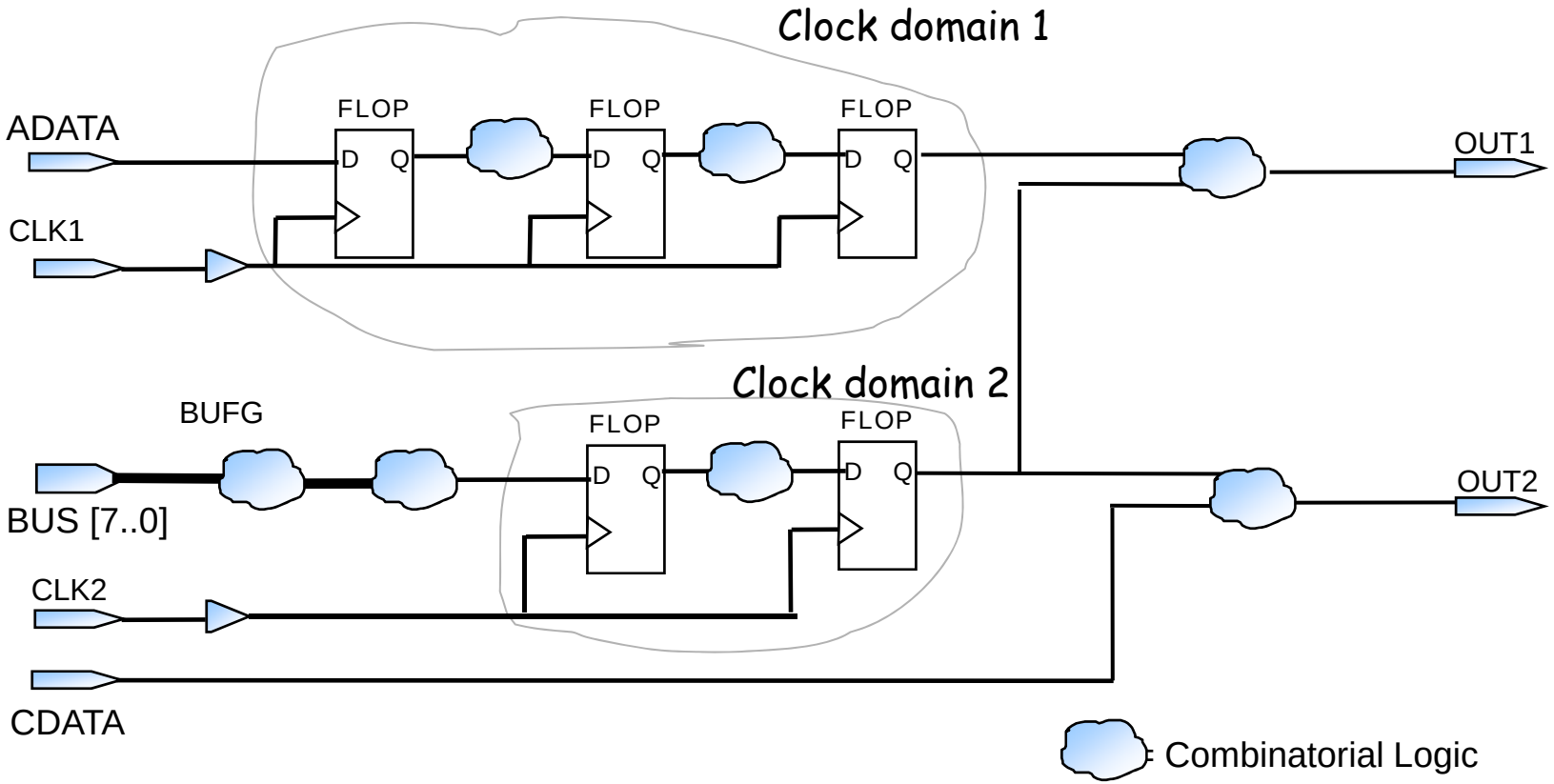
- Mean Time Between Failure: MTBF



The use of synchronizer can significantly reduce Main-Time-Between-Failure (MTBF)

ASIC with Multiple Clock Domains

- A group of circuits that are clocked by the same signal is referred to as a clock domain



Communication Between Different Clock Domains

- Methods for different clock domain communication
  - ✓ Using synchronizer
  - ✓ Using FIFO
  - ✓ Using handshaking protocols