Iraklis Anagnostopoulos

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Iraklis Anagnostopoulos

Research interests

Machine learning: *Approximate computing, heterogeneous hardware accelerators, neural network optimizations, and hardware/software co-design.* **System optimization:** *application customization, power-aware scheduling, memory management.* **Many-core systems:** *Application mapping, network-on-chip architectures, run-time resource management, design and exploration of heterogeneous platforms, and resource contention minimization.*

Education

10/2008 - 02/2014 **Doctor of Philosophy in Electrical and Computer Engineering**, *National Technical University of Athens, Athens, Greece*.
Thesis: Run-time resource management and application customization for many-core embedded platforms.
Advisor: Dimitrios Soudris, Microprocessors and Digital Systems Lab.
Committee: Axel Jantsch, Dimitris Gizopoulos, Kiamal Pekmestzi, Nektarios Kozyris, George Economakos, and Ioannis Papaefstathiou.

09/2008 **Diploma (Master of Science in Engineering) in Electrical and Computer Engineering**, *National Technical University of Athens, Athens, Greece*.
Grade: 8.34/10.
Thesis: Quality of Service (QoS) techniques on Network-on-Chip (NoC).
Advisor: Dimitrios Soudris, Microprocessors and Digital Systems Lab.
Committee: Kiamal Pekmestzi and George Economakos.

Academic employment

05/2021 - Present **Associate Professor**, *Southern Illinois University Carbondale, USA*.
School of Electrical, Computer & Biomedical Engineering.
Director of the Embedded Systems Software Lab.

08/2015 - 05/2021 **Assistant Professor**, *Southern Illinois University Carbondale, USA*.
School of Electrical, Computer & Biomedical Engineering.
Director of the Embedded Systems Software Lab.

Professional employment

07/2013 - 07/2015 **CEO and founder**, *R.D. Software LLC, Greece*.
Start-up focused on acceleration of memory operations for servers. Successfully designed a customized and scalable library to override and accelerate dynamic memory allocation under Linux operating system.

Publications

My own name appears in boldface. Graduate students whose thesis I supervise/ed or whose research I funded, appear in boldface and underlined. Undergraduate students whose thesis I supervise/ed or whose research I funded, appear in boldface and double underlined. The names of industrial collaborators are indicated with †.

Book Editor

E1: B. Candaele, D. Soudris, **I. Anagnostopoulos**. Trusted Computing for Embedded Systems, *Publisher: Springer*, 2015.

Book chapters

B5: G. Zervakis, **I. Anagnostopoulos**, H. Amrouch, J. Henkel. Enabling Efficient Inference of Convolutional Neural Networks via Approximation, in *Approximate Computing, Publisher: Springer*, under editing.

B4: **I. Galanis**, **S. S. N. Perala**, **I. Anagnostopoulos**. Edge Computing and Efficient Resource Management for integration of video devices in Smart Grid deployments, in *In IoT Platforms Targeting Smart-Grid Domain: Design Challenges and Paradigms, Publisher: Springer, Cham*, 2018.

B3: **I. Anagnostopoulos**, S. Xydis, A. Bartzas, Z. Lu, D. Soudris, A. Jantsch. Chapter 8: Middleware Memory Management in NoC, in *Designing 2D and 3D Network-on-Chip Architectures, Publisher: Springer, New York, NY*, 2014.

B2: B. Candaele†, S. Aguirre†, M. Sarlotte†, **I. Anagnostopoulos**, S. Xydis, A. Bartzas, D. Bekiaris, D. Soudris, Z. Lu, X. Chen, J.-M. Chabloz, A. Hemani, A. Jantsch, G. Vanmeerbeeck†, J. Kreku, K. Tiensyrja, F. Ieromnimon†, D. Kritharidis†, A. Wiefrink†, B. Vanthournout, P. Martin. Chapter 11: The MOSART mapping optimization for multi-core ARchiTectures, in *VLSI 2010 Annual Symposium, Publisher: Springer, Dordrecht* 2010.

B1: S. Xydis, A. Bartzas, **I. Anagnostopoulos**, D. Soudris. Chapter 2: Application-Specific Multi-Threaded Dynamic Memory Management, in *Scalable Multi-core Architectures: Design Methodologies and Tools, Publisher: Springer, New York, NY*, 2011.

Referred Journals

J23: **O. Spantidi**, G. Zervakis, **I. Anagnostopoulos** and J. Henkel. Energy-efficient DNN Inference on Approximate Accelerators Through Formal Property Exploration, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2022.

J22: **O. Spantidi**, G. Zervakis, S. Alsalamin, I. R. Ballesteros, J. Henkel, H. Amrouch, **I. Anagnostopoulos**. Targeting DNN Inference via Efficient Utilization of Heterogeneous Precision DNN Accelerators, *IEEE Transactions on Emerging Topics in Computing*, 2022.

J21: **S. Kundan**, **T. Marinakis**, **I. Anagnostopoulos**, D. Kagaris. A Pressure-Aware Policy for Contention Minimization on Multi-core Systems, *ACM Transactions on Architecture and Code Optimization*, 2022.

J20: G. Zervakis, **I. Anagnostopoulos**, S. Salamin, **O. Spantidi**, I. Roman-Ballesteros, Y. Henkel, H. Amrouch. Thermal-Aware Design for Approximate DNN Accelerators, *IEEE Transactions on Computers*, 2022.

J19: N. Irtija, **I. Anagnostopoulos**, G. Zervakis, E.E. Tsiropoulou, H. Amrouch, Y. Henkel. Energy Efficient Edge Computing Enabled by Satisfaction Games and Approximate Computing, *IEEE Transactions on Green Communications and Networking*, 2021.

J18: G. Zervakis, **I. Anagnostopoulos**, S. Salamin, Y. Chauhan, Y. Henkel, H. Amrouch. Impact of NCFET on Neural Network Accelerators, *IEEE Access*, 2021.

J17: **S. Kundan**, **O. Spantidi**, **I. Anagnostopoulos**, C. Nguyen†, G. Bares†. Online Frequency-based Performance and Power Estimation for Clustered Multi-Processor Systems, *Springer Computers & Electrical Engineering*, 2020.

J16: **G. Ioannis**, **I. Anagnostopoulos**, C. Nguyen†, G. Bares†. Efficient Deployment of Spiking Neural Networks on SpiNNaker Neuromorphic Platform, *IEEE Transactions on Circuits and Systems II*, 2020.

J15: **Z. G. Tasoulas**, G. Zervakis, **I. Anagnostopoulos**, H. Amrouch, J. Henkel. Weight-Oriented Approximation for Energy-Efficient Neural Network Inference Accelerators, *IEEE Transactions on Circuits and Systems I: Regular Papers, 2020*.

J14: H. Amrouch, G. Zervakis, S. Salamin, H. Kattan, **I. Anagnostopoulos**, J. Henkel. NPU Thermal Management, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2020.

J13: **I. Galanis**, **S. S. N. Perala**, **L. Kinley**, **I. Anagnostopoulos**. Edge-First Resource Management for Video-based Applications: A Face Detection Use-case, *IEEE Embedded Systems Letters*, 2020.

J12: **T. Marinakis**, **S. Kundan**, **I. Anagnostopoulos**. Meeting Power Constraints while Mitigating Contention on Clustered Multi-Processor Systems, *IEEE Embedded Systems Letters*, 2020.

J11: **T. Marinakis**, **I. Anagnostopoulos**, Performance and Fairness Improvement on CMPs Considering Bandwidth and Cache Utilization, *IEEE Computer Architecture Letters*, 2019.

J10: **Z. G. Tasoulas**, **I. Anagnostopoulos**. Kernel-based Resource Allocation for Improving GPU Throughput while Minimizing the Activity Divergence of SMs, *IEEE Transactions on Circuits and Systems I*, 2019.

J9: **Z. G. Tasoulas**, **I. Anagnostopoulos**. Performance and Aging Aware Resource Allocation for Concurrent GPU Applications under Process Variation, *IEEE Transactions on Nanotechnology*, 2019.

J8: **Z. G. Tasoulas**, **I. Anagnostopoulos**. Improving GPU Performance with a Power-Aware SM Allocation Methodology, *MDPI Electronics*, 2019.

J7: **I. Galanis**, **I. Anagnostopoulos**, P. Gurunathan†, D. Burkard†. Environmental-based speed recommendation for future smart cars, *MDPI Future Internet*, 2019.

J6: **Z. G. Tasoulas**, **I. Anagnostopoulos**, L. Papadopoulos, D. Soudris. A Message-Passing Microcoded Synchronization for Distributed Shared Memory Architectures, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2018.

J5: V. Tsoutsouras, **I. Anagnostopoulos**, D. Masouros, D. Soudris. Hierarchical Distributed Runtime Resource Management scheme for NoC based Many-Cores, *ACM Transactions on Embedded Computing Systems*, 2018.

J4: I. Koutras, **I. Anagnostopoulos**, D. Soudris. Improving Dynamic Memory on Many-Core Embedded Systems With Distributed Shared Memory, *IEEE Embedded System Letters*, 2016.

J3: **I. Anagnostopoulos**, A. Bartzas, I. Filippopoulos, D. Soudris. High-level Customization Methodology for Application-Specific NoC Architectures, *Springer Design Automation for Embedded Systems*, 2013.

J2: **I. Anagnostopoulos**, J.M. Chabloz, I. Koutras, A. Bartzas, A. Hemani, D. Soudris. Power-aware Dynamic Memory Management on May-core Platforms utilizing DVFS, *ACM Transactions on Embedded Computing Systems*, 2013.

J1: **I. Anagnostopoulos**, S. Xydis, A. Bartzas, Z. Lu, D. Soudris, A. Jantsch. Custom Microcoded Dynamic Memory Management for Distributed On-Chip Memory Organizations, *IEEE Embedded Systems Letters*, 2011.

Referred Conferences

C39 (Invited paper): **O. Spantidi**, **I. Anagnostopoulos**. How much is too much error? Analyzing the impact of approximate multipliers on DNN, in *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2022.

C38: **O. Spantidi**, **I. Anagnostopoulos**. Fair Scheduling Through Collaborative Filtering on Multicore Systems, accepted in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2022.

C37: **O. Spantidi**, G. Zervakis, **I. Anagnostopoulos**, H. Amrouch, J. Henkel. Positive/Negative Approximate Multipliers for DNN Accelerators, *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2021.

C36: G. Zervakis, **O. Spantidi**, **I. Anagnostopoulos**, H. Amrouch, J. Henkel. Control Variate Approximation for DNN Accelerators, accepted in *IEEE/ACM Design Automation Conference (DAC)*, 2021.

C35: **S. Kundan**, **I. Anagnostopoulos**. Priority-Aware Scheduling Under Shared-Resource Contention on Chip Multicore Processors, accepted in *International Symposium on Circuits and Systems (ISCAS) IEEE*, 2021.

C34: (Best paper candidate): **O. Spantidi**, **I. Anagnostopoulos**, G. Fainekos. Efficient Resource Management of Clustered Multi-Processor Systems Through Formal Property Exploration, accepted in *Design, Automation, and Test in Europe (DATE) Conference*, 2021.

C33: S. Salamin, G. Zervakis, **O. Spantidi**, **I. Anagnostopoulos**, J. Henkel, H. Amrouch. Reliability-Aware Quantization for Anti-Aging NPUs, accepted in *Design, Automation, and Test in Europe (DATE) Conference*, 2021.

C32: **I. Anagnostopoulos**, D. Kagaris, J. Schmidt†. Prognostics and Health Management Data Handling by Critical Tasks on Multi-Core Platforms, in *Proceedings of IEEE International Conference on Electronics Circuits and Systems (ICECS)*, 2020.

C31: **I. Galanis**, **I. Anagnostopoulos**, C. Nguyen†, G. Bares†, D. Burkard†. Inference and nergy Efficient Design of Deep Neural Networks for Embedded Devices, in *Proceedings of IEEE Computer Society Annual Symposium on VLSI 2020 (ISVLSI)*, 2020.

C30: **O. Spantidi**, **I. Galanis**, **I. Anagnostopoulos**. Frequency-based Power Efficiency Improvement of CNNs on Heterogeneous IoT Computing Systems, in *Proceedings of World Forum on Internet of Things (WFIoT) IEEE*, 2020.

C29: **J. Dickerson**, **I. Galanis**, **Z. G. Tasoulas**, **L. Kinley**, **I. Anagnostopoulos**. Adaptive Approximate Computing on Hardware Accelerators Targeting Internet-of-Things, in *Proceedings of World Forum on Internet of Things (WFIoT) IEEE*, 2020.

C28: K. Poulos, **I. Anagnostopoulos**, T. Haniotakis. ARIAN: A scalable method for **A**dding a**R**b**I**tr**A**ry Numbers on Modern Processors, in *Proceedings of International Symposium on Circuits and Systems (ISCAS) IEEE*, 2020.

C27: **S. Kundan**, **I. Anagnostopoulos**. *"A Machine Learning Approach For Improving Power Efficiency on Clustered Multi-Processor System,* in *Proceedings of International Symposium on Circuits and Systems (ISCAS) IEEE*, 2020.

C26: **I. Galanis**, **T. Marinakis**, **I. Anagnostopoulos**. Workload-aware Management Targeting Multi-Gateway Internet-of-Things, in *Proceedings of IEEE International Conference on Omni-layer Intelligent systems (COINS)*, 2019.

C25 (Best paper candidate): **Z. G. Tasoulas**, **I. Anagnostopoulos**. Optimizing Performance of GPU Applications with SM Activity Divergence Minimization, in *Proceedings of IEEE International Conference on Electronics Circuits and Systems (ICECS)*, 2018.

C24: **M. Mohammad**, **I. Anagnostopoulos**, DROP: Distributed Run-Time and Power Constraint Mapping for Many-Core Systems, in *Proceedings of IEEE International Conference on Electronics Circuits and Systems (ICECS)*, 2018.

C23: **Z. G. Tasoulas**, **R. Guss**, **I. Anagnostopoulos**, *"Performance-based and Aging-aware Resource Allocation for Concurrent GPU Applications,* in *Proceedings of IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, 2018.

C22: **J. S. Koduri**, **I. Anagnostopoulos**, SPA: Simple Pool Architecture for application resource allocation in many-core systems, in *Proceedings of Design, Automation, and Test in Europe (DATE) Conference*, 2018.

C21: **S. R. Punyala**, **T. Marinakis**, A. Komaee, **I. Anagnostopoulos**. Throughput Optimization and Resource Allocation on GPUs under Multi-Application Execution, in *Proceedings of Design, Automation, and Test in Europe (DATE) Conference*, 2018.

C20: **S. S. N. Perala**, **I. Galanis**, **I. Anagnostopoulos**. Fog Computing and Efficient Resource Management in the era of Internet-of-Video Things (IoVT), in *Proceedings of International Symposium on Circuits and Systems (ISCAS) IEEE*, 2018.

C19: **I. Galanis**, P. Gurunathan†, D. Burkard†, **I. Anagnostopoulos**. Weather-based road condition estimation in the era of Internet-of-Vehicles (IoV), in *Proceedings of International Symposium on Circuits and Systems (ISCAS) IEEE*, 2018.

C18: **D. Olsen**, **I. Anagnostopoulos**, *"Performance-aware resource management of multi-threaded applications on many-core systems,* in *Proceedings of ACM Great Lakes Symposium on VLSI (GLSVLSI) conference*, 2017.

C17: **T. Marinakis**, A. H. Haritatos, K. Nikas, G. Goumas, **I. Anagnostopoulos**. An Efficient and Fair Scheduling Policy For Multiprocessor Platforms, in *Proceedings of International Symposium on Circuits and Systems (ISCAS) IEEE*, 2017.

C16: **S. Behroozi**, **I. Anagnostopoulos**, Application Resource Management for Exploitation of Non-Volatile Memory in Many-Core Systems, in *Proceedings of International Symposium on Circuits and Systems (ISCAS) IEEE*, 2017.

C15: **I. Galanis**, **D. Olsen**, **I. Anagnostopoulos**. A multi-agent based system for run-time distributed resource management, in *Proceedings of International Symposium on Circuits and Systems (ISCAS) IEEE*, 2017.

C14: T. Melissaris, **I. Anagnostopoulos**, D. Soudris, D. Reisis, Agora: Agent and Market-Based Resource Management for Many-Core systems, in *Proceedings of IEEE International Conference on Electronics Circuits and Systems (ICECS)*, 2016.

C13: K. Gyftakis, **I. Anagnostopoulos**, D. Soudris, D. Reisis, A MapReduce framework implementation for Network-on-Chip platforms, in *Proceedings of IEEE International Conference on Electronics Circuits and Systems (ICECS)*, 2014.

C12: **I. Anagnostopoulos**, V. Tsoutsouras, A. Bartzas, D. Soudris. Distributed run-time resource management for malleable applications on many-core platforms, in *Proceedings of Design Automation Conference (DAC)*, 2013.

C11: **I. Anagnostopoulos**, A. Bartzas, G. Kathareios, D. Soudris. A Divide and Conquer based Distributed Run-time Mapping Methodology for Many-Core platforms, in *Proceedings of Design, Automation, and Test in Europe (DATE) Conference*, 2012.

C10 (Invited Paper) K. Siozios, D. Diamantopoulos, I. Kostavelis, E. Boukas, L. Nalpantidis, D. Soudris, A. Gasteratos, M. Aviles, **I. Anagnostopoulos**. SPARTAN project: Efficient implementation of computer vision algorithms onto reconfigurable platform targeting to space applications, in *Proceedings of the 6^{th} International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*, 2011.

C9 (Invited Paper) C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, JM. Zins, H. Hubert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, **I. Anagnostopoulos**, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, J. Ansari, P. Mahonen, B. Vanthournout. Parallel programming and run-time resource management framework for many-core platforms: The 2PARMA approach, in *Proceedings of the 6^{th} International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*, 2011.

C8 (Invited Paper) A. Bartzas, P. Bellasi, **I. Anagnostopoulos**, C. Silvano, W. Fornaciari, D. Soudris, D. Melpignano, C. Ykman-Couvreur. Runtime Resource Management Techniques for Many-core Architectures: The 2PARMA Approach, in *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, 2011.

C7: K. Siozios, **I. Anagnostopoulos**, D. Soudris, Multiple Vdd on 3D NoC Architectures, in *Proceedings of 17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, 2010.

C6: S. Xydis, A. Bartzas, **I. Anagnostopoulos**, D. Soudris, K. Pekmestzi. Custom Multi-Threaded Dynamic Memory Management for Multiprocessor System-on-Chip Platforms, in *Proceedings of International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)*, 2010.

C5: (Invited Paper) B. Candaele[†], S. Aguirre[†], M. Sarlotte[†], **I. Anagnostopoulos**, S. Xydis, A. Bartzas, D. Bekiaris, D. Soudris, Z. Lu, X. Chen, J.-M. Chabloz, A. Hemani, A. Jantsch, G. Vanmeerbeeck[†], J. Kreku, K. Tiensyrja, F. Ieromnimon[†], D. Kritharidis[†], A. Wiefrink[†], B. Vanthournout, P. Martin, Mapping Optimisation for Scalable multi-core ARchiTecture: The MOSART approach, in *Proceedings of IEEE Computer Society Annual Symposium on VLSI (IS-VLSI)*, 2010.

C4: I. Filippopoulos, **I. Anagnostopoulos**, A. Bartzas, D. Soudris, G. Economakos. Systematic Exploration of Energy-Efficient Application-Specific Network-on-Chip Architectures, in *Proceedings of IEEE Computer Society Annual Symposium on VLSI (IS-VLSI)*, 2010.

C3: K. Siozios, **I. Anagnostopoulos**, D. Soudris. A High-Level Mapping Algorithm Targeting 3D NoC Architectures with Multiple Vdd, in *Proceedings of IEEE Computer Society Annual Symposium on VLSI (IS-VLSI),* 2010.

C2: **I. Anagnostopoulos**, A. Bartzas, D. Soudris, Application-Specific Temperature Reduction Systematic Methodology for 2D and 3D Networks-on-Chip, in *Proceedings of International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 2009.

C1: **I. Anagnostopoulos**, A. Bartzas, I Vourkas, D. Soudris, Node Resource Management for DSP Applications on 3D Network-on-Chip architectures, in *Proceedings of 16th International Conference on Digital Signal Processing (DSP)*, 2009.

Other Publications

O8: I. Galanis, D. Olsen, **I. Anagnostopoulos**. Hydra: A distributed run-time management framework for multi-agent systems, in *EnESCE: Workshop on Energy-efficient Servers for Cloud and Edge Computing, HiPEAC*, 2017.

O7: S. Xydis, **I. Anagnostopoulos**, A. Bartzas, D. Soudris. Dynamic Memory Management Customization for Multi-Processor Systems-on-Chip, in *University Booth, Design, Automation, and Test in Europe (DATE) Conference*, 2010.

O6: S. Xydis, **I. Anagnostopoulos**, A. Bartzas, D. Soudris, G. Economakos. Dynamic Memory Management Customization for Multi-Processor Systems-on-Chip, in *Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Tools, and Applications, Design, Automation, and Test in Europe (DATE) Conference*, 2010.

O5: **I. Anagnostopoulos**, K. Siozios, D. Soudris, Microcoded Dynamic Memory allocation for Multi-core Networks-on-Chip, *HiPEAC ACACES summer school*, 2010.

O4: I. Filippopoulos, **I. Anagnostopoulos**, A. Bartzas, D. Soudris, G. Economakos. Temperature-Aware Platfrom Optimizations for 2D and 3D Networks-on-Chip, *4th National Conference of Electrical and Computer Engineering*, 2010.

O3: **I. Anagnostopoulos**, K. Siozios, D. Soudris. 3D Networks-on-Chip: Architectures and tools, *HiPEAC ACACES summer school*, 2009.

O2: **I. Anagnostopoulos**, A. Bartzas, D. Soudris, Temperature-Aware Platfrom Optimizations for 2D and 3D Networks-on-Chip, *3rd National Conference of Electrical and Computer Engineering*, 2009.

O1: A. Bartzas, **I. Anagnostopoulos**, K. Siozios, D. Soudris, Topology Exploration and Buffer Sizing for Three-Dimensional Networks-on-Chip, in *Workshop of 3D Integration, Design, Automation, and Test in Europe (DATE) Conference*, 2009.

Research Projects - Grants

- **Active research programs**, Assistant Professor, Southern Illinois University Carbondale, U.S.A.

01/2022 - 12/2022 **Enhancing synergistic execution of neural networks with joint pruning and mixed precision quantization, Single PI: I. Anagnostopoulos**, *Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Ford Motor Company. **Total amount: $50,000**.
Brief Description: Chip multiprocessors (CMPs) have become dominant in the automotive industry as they accommodate an increasing amount of cores in order to satisfy the increasing demands of the complicated services provided by modern vehicles. Additionally, heterogeneity has been introduced to combine performance and functional divergent offering significant computing power with more flexible power-performance trade-offs. As more and more services depend on concurrent execution of multiple neural networks, this multi-application execution environment on modern systems creates interference delays leading in violation of time constraints. In this project, we will extend the framework for synergistic execution developed last year, to further optimize the execution of neural networks by supporting joint pruning and mixed precision quantization.

01/2022 - 12/2022 **Determinism of Critical Tasks on Multi-Core Platforms in the Presence of PHM Data Operations (project continuation),**, *PI: **I. Anagnostopoulos**; co-PI: D. Kagaris, Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Collins Aerospace. **Total amount: $50,000**.
Brief Description: Prognostics and health management (PHM) data are collected on site but have to be eventually off-loaded to the cloud for further processing for predictive maintenance purposes. At the same time, the controllers of the system components should continue their operation unaffected by the PHM data collection and transmission. In this project, we plan to extend the framework built in the previous years in order to support more sophisticated functions and benchmark the effect of different services. Particularly, we will focus on the investigation of different FreeRTOS versions and compare their deterministic behavior against Linux with real-time kernel over a bare-metal hypervisor.

- **Completed research programs**, Assistant Professor, Southern Illinois University Carbondale, U.S.A.

01/2021 - 12/2021 **Enhancing vehicular applications using adaptive and synergistic resource management, Single PI: I. Anagnostopoulos**, *Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Ford Motor Company. **Total amount: $50,000**.
Brief Description: Chip multiprocessors (CMPs) have become dominant in the automotive industry. Additionally, heterogeneity has been introduced to combine performance and functional divergent offering significant computing power with more flexible power-performance trade-offs. As more and more services depend on concurrent execution of multiple neural networks, this multi-application execution environment on modern systems creates interference and delays leading in violation of time constraints. In this project, we will investigate and develop a service oriented architecture in order to allow synergistic resource management of neural networks on heterogeneous CMPs.

01/2021 - 12/2021 **Heterogeneity-aware orchestration and efficient utilization of modern many-core systems, Single PI: I. Anagnostopoulos**, *Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Intel. **Total amount: $50,000**.
Brief Description: When applications run concurrently on a CMP, they compete for shared resources, such as Last Level Cache (LLC) and main memory bandwidth. Conventional design approaches and industry trends are application agnostic. They mostly try to maximize consistency offering generic solutions and ignoring the requirements of diverse applications. In this project, we propose a two-step methodology to orchestrate the executing and resource allocation of modern CMPs. The goal of the first step is to estimate the performance of different applications on platform with different architecture, while avoiding exhaustive application profiling. The second step focuses on the automatic generation of performance estimators and resource allocation policies to be integrated into the scheduler so as to maximize the system utilization for specific workloadsi.

01/2021 - 12/2021 **Determinism of Critical Tasks on Multi-Core Platforms in the Presence of PHM Data Operations,**, *PI: **I. Anagnostopoulos**; co-PI: D. Kagaris, Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Collins Aerospace. **Total amount: $50,000**.
Brief Description: Prognostics and health management (PHM) data are collected on site but have to be eventually off-loaded to the cloud for further processing for predictive maintenance purposes. At the same time, the controllers of the system components should continue their operation unaffected by the PHM data collection and transmission. In this proposal, which is based on the infrastructure that we have already built in the 2019 project, we investigate the effect of different multi-core configurations to provide PHM capability to an embedded system without impacting its performance. Additionally, we will explore the impact of data management services (e.g., encryption, compression, filtering) to the overall deployment in terms of deterministic behavior.

05/2019 - 06/2021 **Modular and scalable infrastructure for the SIUC campus**, *PI: S. Tragoudas; co-PIs: **I. Anagnostopoulos**, A. Baduge, C. Hatziadoniu, A. Komaee, H. Wang, Funding source: Illinois Environmental Agency/US Department of Energy*. **Total amount: $1,008,000 ($900,000.00 from the IEPA/USDOE and $108,000.00 matching from SIUC)**.
Brief Description: Implement a scalable infrastructure consisting of photovoltaic (PV) panels and energy storage units to generate electricity in normal conditions and function as a backup power source in case of electricity outage. In the events of power outage, it will sustain the operation of a computing and control room in Engineering Building E as well as a wireless communication infrastructure. With this infrastructure and data obtained from its operation, the project intends to demonstrate that PV systems with energy storage provide a viable alternative to traditional diesel powered generators when selecting backup power sources for small-scale applications. In addition, the project will develop solar powered LTE communication modules to sustain cellular communication for emergency responders in the events of natural disasters that cause outages of both power and cellular service.

01/2020 - 12/2020 **Real-time Deep Learning System on FPGA platforms for Autonomous Vehicle Applications**, *PI: H. Wang; co-PIs: **I. Anagnostopoulos**, S. Tragoudas, Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Ford Motor Company. **Total amount: $50,000**.
Brief Description: This project investigates benefits and challenges on implementing deep learning algorithms on state-of-the-art FPGA and GPU hardware platforms for real-time image classifications for autonomous vehicle applications. The two platforms will be compared in terms of toolchain complexity, inference accuracy, throughput, and power consumption.

08/2019 - 07/2020 **Enhancing and Protecting Vehicular Applications Using Isolation and Adaptive Offloading, Single PI: I. Anagnostopoulos**, *Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Ford Motor Company. **Total amount: $50,000**.
Brief Description: The focus of this project is to develop techniques for enhancing and protecting vehicular applications using isolated application execution combined with transparent and adaptive task offloading. The first pillar is the application isolation in order to increase performance and meet time-requirements of automotive services. The second pillar is the trade-off estimation of task offloading as a way to further enhance quality of service, while the third pillar is the isolation of the applications increasing data integrity. The overall goal is to develop a unified design methodology and framework that will speed up and secure the content delivery and analysis process at the vehicle edge by using process isolation and task offloading.

08/2019 - 07/2020 **Enhancing QoS of Mixed Criticality Workloads on Modern Many-core Systems, Single PI: I. Anagnostopoulos**, *Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Intel. **Total amount: $50,000**.
Brief Description: The fact that cores share architectural components, such as caches and memory controllers, results in severe performance degradation. State-of-art approaches balance the applications' accesses to the shared resources by splitting equally the CPU time. Even though this policy is fair regarding the CPU time that each application gets, it does not take into consideration any contention effects that affect their performance. The focus of this project is to develop a four-step approach in order to (i) offer QoS guarantees by ensuring that high priority tasks and applications have minimal interference, and (ii) investigate the limitations of different Intel processor microarchitectures in order to offer such QoS guarantees.

08/2019 - 07/2020 **Prognostics and Health Management (PHM)-Enabled Real-Time Embedded Architectures,**, *PI: **I. Anagnostopoulos**; co-PI: D. Kagaris, Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Collins Aerospace. **Total amount: $50,000**.
Brief Description: Machinery (whether used in airplanes, automobiles, industrial machines, etc.) is inevitably subject to wear and needs to be maintained. Corrective maintenance, in which a component is replaced only after it has failed, is inapplicable/unacceptable in many cases where failures are catastrophic. Data-driven predictive maintenance is the smart way to do maintenance, but the collection of the PHM data should interfere the least with the controllers' operation. The effect of different multicore architectures (core assignment, partition assignment) to provide PHM capability to an embedded system without impacting its performance need to be investigated.

04/2019 - 08/2020 **Parameter exploration and adversarial learning on Loihi**, *PI:* ***I. Anagnostopoulos****; co-PI: S. Tragoudas; Funding source: Intel*. Access to the Intel Loihi Development System (direct and remote access)

Brief Description: Classification accuracy and the effectiveness of certain adversarial learning approaches depend on the underlying hardware platform because many automotive applications impose power dissipation and performance constraints. Certain hyperparameters relate directly to power and performance. In particular, the number of neurons per layer when coupled with the number of layers relates to power dissipation, while the number of layers relates to performance. Therefore, training algorithms will consider constraints on these hyperparameters in order to satisfy power and performance constraints. In order for the proposed approach to be effective in classification accuracy and also in design time efficiency, accurate platform-specific models must be developed to estimate power and delay per neuron. We will also investigate whether optimum solutions should be proposed directly on SNN or proceed as in and first derive an optimum CNN topology and then map it to SNN.

08/2018 - 07/2019 **Impact of Artificial Neural Network architectures on autonomous driving, Single PI: I. Anagnostopoulos**, *Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Ford Motor Company. **Total amount: $50,000**.

Brief Description: The rapid growth of on-vehicle multi-sensor inputs along with off-vehicle data streams provides an opportunity for developing innovative applications and services for modern vehicles. Autonomous cars employ hundreds of sensors for situational and environmental information and in order to integrate such services, new programming models and hardware infrastructure have been introduced. From the application perspective, machine learning algorithms have been utilized in order to further enhance the decision making process of autonomous vehicles. Image, speech and data classification are some examples where Artificial Neuron Networks (ANNs) prevail as the solution due to the complexity of the problem. In this project, we investigate the trade-offs of modern ANNs on embeded devices and the integration of neuromorphic platforms in smart cars.

08/2017 - 07/2018 **Service oriented architecture and application optimizations for smart cars, Single PI: I. Anagnostopoulos**, *Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Ford Motor Company. **Total amount: $40,000**.

Brief Description: Modern cars employ hundreds of sensors for situational and environmental information and in order to integrate such services, new programming models and hardware infrastructure have been introduced. The project focuses on application optimization and development of service-oriented communication for seamless integration with regular automotive systems. Specifically, interfaces are being developed that will allow the communication of RTOS-based systems with more sophisticated software architectures and tools.

08/2016 - 07/2017 **Internet-of-Things Applications Development for private LTE small-cell networks,**, *PI:* ***I. Anagnostopoulos****; co-PI: A. Baduge, Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Lemko Corporation. **Total amount: $35,000**.

Brief Description: We are witnessing the dawn of a new era of Internet of Things (IoT; also known as Internet of Objects). Generally speaking, IoT refers to the networked interconnection of everyday objects, which are often equipped with ubiquitous intelligence. Smart building, self-driving cars, house monitoring and management, city electricity and pollution monitoring are some examples where dynamic networked real-time systems are deployed. This bloom of dynamic networked devices was also a result of new network services. With lower latency and higher bandwidth than its predecessor 3G networks, the latest cellular technology 4G LTE has been attracting many new users. However, the interactions among applications and network transport protocol still remain unexplored. In this project, we propose methodologies for interfacing, controlling and monitoring IoT devices in industrial settings over private LTE small-cell networks over 3.65 GHz frequency band.

08/2016 - 07/2017 **Environmental information and multi-sensor data fusion based performance estimations for smart cars, Single PI: I. Anagnostopoulos**, *Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Ford Motor Company. **Total amount: $50,000**.

Brief Description: The rapid growth of on-vehicle multi-sensor inputs along with off-vehicle data streams provides an opportunity for innovation in real-time decision making. The development of new advanced sensors is not sufficient enough without the utilization of enhanced signal processing techniques such as the data fusion methods. Multi-sensor data fusion (MSDF) is the process of combining or integrating measured or preprocessed data or information originating from different active or passive sensors. In this project, we develop and explore state-of-art data fusion techniques for decision making for automotive applications. Specifically we combine the benefits offered by car's increased connectivity (e.g. Internet, cloud services) with on-vehicle sensor information for providing detailed information about the state of the car and the environment.

08/2015 - 07/2016 **Distributed Run-time Management for Multi-agent System, Single PI: I. Anagnostopoulos**, *Funding source: NSF I/UCRC Consortium for Embedded Systems (CES)*. Main supporting CES industry member: Ford Motor Company. **Total amount: $50,000**.

Brief Description: Today's prevalent solutions for modern multi-agent systems employ many processing inter-connected units leaving behind complex centralized approaches. Especially in modern automotive systems where high numbers of electronic components are employed. Navigation, car security, infotainment, travel information etc. are services highly depended on modern computing systems. In this project, we couple the concept of multi-agent systems with run-time resource management techniques in order to develop a distributed framework for run-time management of multi-agent systems.

- **Completed research programs**, research assistant, National Technical University of Athens, Athens, Greece.

03/2015 - 07/2015 **AEGLE: An Analytics Framework for Integrated and Personalized Healthcare Services in Europe**. H2020-ICT-2014-1. Researcher: Defining system requirements and scenarios of use.
Partners: Exodus, S.A., Institute of Communication and Computer Systems, Kingston University Higher Education Corporation, Centre for Research and Technology Hellas, MAXELER Technologies, Uppsala University, University Vita-Salute San Raffaele, TML, Erasmus Universiteit Rotterdam, Croydon Health Services NHS Trust, LOBA, University Hospital of Heraklion, Gnubila.

01/2011 - 03/2014 **TOISE: Trusted Computing for European Embedded Systems**. IST-282557-2. Principal Researcher: Responsible for dynamic memory management in trusted computing platforms.
Partners: THALES, STMicroelectronics (Rousset), GEMALTO SA, CEA Leti, EADS CASSIDIAN SAS, EADS France Innovation Works SAS, Institut Telecom ParisTech, Secure-IC, Magillem Design Systems, STMicroelectronics Srl, AZCOM Technology, Politecnico di Milano, Numonyx Srl, Università di Milano Bicocca, Proton World International NV, Hellenic Aerospace Industry, Institute of Communication and Computer Systems, Agencia Consejo Superior de Investigaciones Científicas,Tecnologías Servicios Telemáticos y Sistemas S.A., Universidad de Cantabria.

03/2010 - 12/2012 **2PARMA: Parallel Paradigms and Run-time Management Techniques for Many-core Architectures**. FP7-ICT-2009-4-248716. Researcher: Responsible for run-time resource management in multi-core platforms. Workpackage 4: Run-Time Management.
Partners: Politecnico di Milano, STMicroelectronics, Fraunhofer Institut for Telcommunications / Heinrich-Hertz Institut, IMEC, Institute of Communication and Computer Systems, RWTH Aachen University, CoWare.

01/2008 - 12/2010 **MNEMEE: Memory Management Technology for Adaptive and Efficient Design of Embedded Systems**. IST-216224. Researcher: Responsible for dynamic memory management in embedded systems. Workpackage 2: Source-to-Source Optimizations of Dynamically Allocated Data Mapping on MPSoC Platforms.
Partners: IMEC, NTUA, Technical University of Eindhoven, Informatik Centrum Dortmund e.V., Intracom, THALES.

09/2009 - 12/2009 **Invited Researcher**, *KTH Royal Institute of Technology, Stockholm, Sweden*. Build a dynamic memory management library in microcode targeting performance efficiency..

09/2008 - 12/2009 **MOSART: Mapping Optimization for Scalable multi-core ARchiTecture**. IST-215244. Researcher: Responsible for dynamic memory management for DSM platforms. Workpackage 2: Data Storage Optimization and Middleware.
Partners: THALES, NTUA, KTH, IMEC, VTT, Intracom, Coware, Arteris.

Awards

- *Outstanding Teacher of the year in the Department of Electrical & Computer Engineering*, Southern Illinois University Carbondale, 2018.
- *Distributed Run-time Management for Multi-agent Systems* was Selected by NSF to be part of the "Industry-Nominated Technology Breakthroughs", 2016.
- HiPEAC Paper Award: Design Automation Conference, Austin, Texas, 2013.
- 3^{rd} Best paper award: 4^{th} National Conference of Electrical and Computer Engineering, 2010, Patra, Greece.

- HiPEAC Grant for HiPEAC summer school, Barcelona, Spain, 2009.

Students

Current Ph.D. students

- Andreas Karatzas (Full time student starting Spring 2022)
  Research: *Approximate computing in modern accelerators.*
- Ourania Spantidi (Full time student since Fall 2019)
  Research: *Optimization of neural networks in edge computing.*

Current M.Sc. students

- Shaleen Acharya (Full time student starting Spring 2022)
  Research: *Quantization and synergistic execution of neural networks on embedded devices.*

Alumni Ph.D. students

- Zois Gerasimos Tasoulas
  Research: *Resource Management and application customization for hardware accelerated systems.*
  First placement: NVIDIA, USA
- Ioannis Galanis
  Dissertation: *Resource management in edge computing for Internet of Things.*
  First placement: Intel, USA
- Theodoros Marinakis
  Dissertation: *Enhancing Fairness And Performance On Chip Multi-processor Platforms With Contention-aware Scheduling Policies.*
  First placement: NVIDIA, USA

Alumni M.Sc. students

- Anish Ghimire
  Thesis: *Optmization of asymmetric many-core systems.*
  First placement: Qualcomm, USA
- Shraddha Dahal
  Thesis: *Synergistic execution of Neural Networks on modern embedded systems.*
  First placement: Qualcomm, USA
- Saroj Sapkota
  Thesis: *Efficient Resource Management on Embedded Devices Via Isolation and Adaptive Resource Allocation.*
  First placement: Intel, USA
- Jonathan Dickerson
  Thesis: *Supporting Approximate Computing on Coarse Grained Re-configurable Array Accelerators.*
- Srinivasa Reddy Punyala
  Thesis: *Throughout Optimization and Resource Allocation on GPUs under multi-application execution.*

- Sai Saketh Nandan Perala
  Thesis: *Efficient Resource Management for Video Applications in the Era of Internet-of-Things (IoT).*
  First placement: Fiat Chrysler Automobile, USA
- Jayasimha sai Koduri
  Thesis: *Simple Pool Architecture for Application Resource Allocation in Many-Core Systems.*
  First placement: Qualcomm, USA
- Daniel Olsen
  Thesis: *Performance-Aware Resource Management of Multi-Threaded Applications for Many-Core Systems.*
  First placement: Boeing, USA
- Mohammad Essa Mohammad
  Thesis: *Distributed Run-Time and Power Constraints Mapping for Many-Core Systems.*

Ph.D. Thesis committee member

- Puneet Savanur, School of Electrical, Computer and Biomedical Engineering, SIU, 2022. Chair: Dr. S. Tragoudas. *Dissertation: Techniques to Address Manufacturing Defects in Deep Sub-micron.*
- Diluka A Loku Galappaththige, School of Electrical, Computer and Biomedical Engineering, SIU, 2021. Chair: Dr. G. Baduge. *Dissertation: Cell-free and Intelligent Reflective Surfaces Aided Architectures for Wireless Communications.*
- Konstantinos Poulos, School of Electrical and Computer Engineering, SIU, 2020. Chair: Dr. T. Haniotakis. *Dissertation: New Techniques on VLSI Testing & Efficient Implementation of Arithmetic Operations.*
- Pavan Kumar Javvaji, School of Electrical and Computer Engineering, SIU, 2019. Chair: S. Tragoudas. *Dissertation: Testing and Security Considerations in Presence of Process Variations.*
- Ning Yang, School of Electrical and Computer Engineering, SIU, 2019. Chair: K. Chen, *Dissertation: Efficient and Secure Named Data Networking for Connected Vehicles.*
- Seyed Nima Mozaffari Mojaveri, School of Electrical and Computer Engineering, SIU, 2017. Chair: Dr. S. Tragoudas. *Dissertation: Design and Test of Digital Circuits and Systems Using CMOS and Emerging Resistive Devices.*
- Cheng-Liang Hsieh, School of Electrical and Computer Engineering, SIU, 2016. Chair: Dr. N. Weng. *Dissertation: Design and Implementation of Scalable High-Performance Network Functions.*
- Sourav Dutta, School of Electrical and Computer Engineering, SIU, 2016. Chair: Dr. D. Kagaris. *Dissertation: Performance Estimation and Scheduling for Parallel Programs with Critical Sections.*

Master Thesis committee member

- Mohammad Reza Shariatmadari , School of Electrical, Computer & Biomedical Engineering, SIU, 2021. Chair: A. Komaee. *Thesis: Feedback Control and Stability Analysis of a Permanent Levitation System .*
- Prashant Baral, School of Electrical, Computer & Biomedical Engineering, SIU, 2021. Chair: N. Weng. *Thesis: IoT Device Identification using Device Fingerprint and Deep Learning.*

- Aashish Itani, School of Electrical, Computer & Biomedical Engineering, SIU, 2021. Chair: S. Tragoudas. *Thesis: Comparison of Adversarial Attack on traditional and Spiking Neural Networks.*
- Luis Rodrigo Tituana Davila, School of Electrical and Computer Engineering, SIU, 2020. Chair: A. Komaee. *Thesis: Implementation of a Planar Magnetic Manipulator with Rotatable Permanent Magnets.*
- Imran Khan, School of Electrical and Computer Engineering, SIU, 2020. Chair: K. Chen. *Thesis: Efficient MPTCP-based Multipath Network Access for Connected Vehicles.*
- Joseph Leo, Thesis Defense, School of Electrical and Computer Engineering, SIU, 2019. Chair: H. Wang. *Thesis: Design of a Wireless Sensor Platform with Energy Harvesting.*
- Jessica Suda, School of Electrical and Computer Engineering, SIU, 2019. Chair: D. Kagaris. *Thesis: Misfire-Fault Classification for Future On-Board Diagnostics III Vehicle.*
- Claudio Copello, School of Electrical and Computer Engineering, SIU, 2016. Chair: Dr. N. Weng. *Thesis: Enhancing Data Security and Energy Efficiency on Batter-Free Programmable Platform via Adaptive Scheduling.*

Senior design projects

- *Integrated Surface Vehicle Design Challenge*, 2015-16.
- *Voice-Controlled Autonomous Vehicle*, 2015-16.
- *Microsoft Hololens Virtualized environment*, 2016-17.
- *HoloLens Internet-of-Things Smart Room*, 2017-18.
- *Video streaming over Hololens*, 2017-18.
- *Face detection in augmented reality*, 2017-18.
- *Analyze basketball game and provide statistics with augmented reality*, 2018-19.
- *Boeing senior design group*, 2019-20.
- *Park EZ*, 2019-20.
- *Boeing senior design group*, 2020-21.
- *Dashboard for data analyticis on SIU infrastructure*, 2020-21.

Teaching

Spring 2022 Instructor undergraduate course *"ECE 329 - Computer Organization & Design"*, School of Electrical and Computer Engineering, SIU.

Spring 2022 Instructor undergraduate course *"ECE 430 - Systems Programming"*, School of Electrical, Computer and Biomedical Engineering, SIU.

Fall 2021 Instructor undergraduate course *"ECE 432 - Parallel Programming"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.2/5, Instructor: 4.25/5, Responses: 1/9.

Fall 2021 Instructor undergraduate course *"ECE 329 - Computer Organization & Design"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.2/5, Instructor: 5/5, Responses: 1/9.

Spring 2021 Instructor undergraduate course *"ECE 321 - Introduction to Software Engineering"*, School of Electrical, Computer and Biomedical Engineering, SIU.
Evaluation: Course: 2.72/5, Instructor: 2.95/5, Responses: 5/16.

Spring 2021 Instructor undergraduate course *"ECE 430 - Systems Programming"*, School of Electrical, Computer and Biomedical Engineering, SIU.
Evaluation: Course: 3.6/5, Instructor: 4.25/5, Responses: 4/13.

Fall 2020 Instructor graduate course *"ECE 532 - Programming for Parallel Processors"*, School of Electrical, Computer and Biomedical Engineering, SIU.
Evaluation: Course: 4.75/5, Instructor: 5/5, Responses: 8/9.

Spring 2020 Instructor graduate course *"ECE 536 - Many-core embedded systems"*, School of Electrical, Computer and Biomedical Engineering, SIU.
Evaluation: Course: 4.8/5, Instructor: 5/5, Responses: 4/7.

Spring 2020 Instructor undergraduate course *"ECE 430 - Systems Programming"*, School of Electrical, Computer and Biomedical Engineering, SIU.
Evaluation: Course: 4.3/5, Instructor: 4.5/5, Responses: 4/19.

Fall 2019 Instructor undergraduate course *"ECE 432 - Parallel Programming"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.5/5, Instructor: 4.6/5, Responses: 8/23.

Fall 2019 Instructor graduate course *"ECE 532 - Programming for Parallel Processors"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 5/5, Instructor: 5/5, Responses: 2/3.

Fall 2019 Instructor undergraduate course *"ECE 321 - Introduction to Software Engineering"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.6/5, Instructor: 4.4/5, Responses: 5/13.

Spring 2019 Instructor undergraduate course *"ECE 321 - Introduction to Software Engineering"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.33/5, Instructor: 4.33/5, Responses: 18/20.

Fall 2018 Instructor undergraduate course *"ECE 432 - Parallel Programming"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.62/5, Instructor: 4.76/5, Responses: 17/21.

Fall 2018 Instructor graduate course *"ECE 532 - Programming for Parallel Processors"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.71/5, Instructor: 5/5, Responses: 7/7.

Fall 2018 Instructor undergraduate course *"ECE 321 - Introduction to Software Engineering"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.45/5, Instructor: 4.70/5, Responses: 20/23.

Spring 2018 Instructor undergraduate course *"ECE 321 - Introduction to Software Engineering"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.56/5, Instructor: 4.44/5, Responses: 9/12.

Fall 2017 Instructor undergraduate course *"ECE 321 - Introduction to Software Engineering"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 5/5, Instructor: 5/5, Responses: 5/8.

Fall 2017 Instructor undergraduate course *"ECE 432 - Parallel Programming"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.82/5, Instructor: 4.82/5, Responses: 11/19.

Fall 2017 Instructor graduate course *"ECE 532 - Programming for Parallel Processors"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.75/5, Instructor: 4.50/5, Responses: 4/4.

Spring 2017 Instructor graduate course *"ECE 536 - Real-time Embedded Systems"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 5/5, Instructor: 4.82/5, Responses: 11/13.

Spring 2017 Instructor undergraduate course *"ECE 430 - Principles of System programming"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.53/5, Instructor: 4.58/5, Responses: 19/24.

Fall 2016 Instructor undergraduate course *"ECE 321 - Introduction to Software Engineering"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.50/5, Instructor: 4.19/5, Responses: 16/25.

Fall 2016 Instructor undergraduate course *"ECE 432 - Parallel Programming"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.33/5, Instructor: 4.60/5, Responses: 15/19.

Fall 2016 Instructor graduate course *"ECE 532 - Programming for Parallel Processors"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 5/5, Instructor: 4.90/5, Responses: 10/10.

Spring 2016 Instructor crosslisted course *"ECE 493/593 - Special Topics in Electrical Engineering - Principles of System programming"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.44/5, Instructor: 4.67/5, Responses: 9/19.

Fall 2015 Instructor undergraduate course *"ECE 321 - Introduction to Software Engineering"*, School of Electrical and Computer Engineering, SIU.
Evaluation: Course: 4.18/5, Instructor: 4.50/5, Responses: 17/20.

2010-2014 Teaching assistant *"Embedded Systems"*, Semester 9^{th}, School of Electrical and Computer Engineering, NTUA.

2009-2013 Lab assistant *"Microprocessors Lab"*, Semester 7^{th}, School of Electrical and Computer Engineering, NTUA.

2009-2011 Lab assistant *"Digital VLSI systems"*, Semester 8^{th}, School of Electrical and Computer Engineering, NTUA.

Service

University service

- SIU Graduate Council Committee Member, 2021 - 2024.
- Graduate Committee member of School of Electrical, Computer and Biomedical Engineering, 2021.
- Computer Engineering Committee member of School of Electrical, Computer and Biomedical Engineering, 2021.

Community service

- Special Session organizer: *Approximate Computing: From circuit design to system integration*, IEEE International Symposium on Quality Electornic Design (ISQED) 2022.

- Invited Session organizer: *Approaches and Methods for Monitoring and Management of Edge Computing Systems and Networks*, IEEE International Conference on High Performance Switching and Routing (HPSR) 2022.
- Review Editor on the Editorial Board of Frontiers in Communications and Networks journal.
- Member of IEEE CAS Sensory Systems Technical Committee (SSTC).
- Member of IEEE CAS Multimedia Systems & Applications Technical Committee (MSATC).
- IEEE Industry Applications Society (IAS) as IEEE IAS CMD Thesis Contest Evaluator.

Conference Program Committee

2023:

- ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), Technical Program Committee Member.

2022:

- ACM/IEEE Design Automation Conference (DAC), AI/ML System Design, Technical Program Committee Member.
- ACM Great Lakes Symposium on VLSI (GLSVLSI), VLSI Design Track, Technical Program Committee Member.
- IEEE Global Communications Conference: Green Communication Systems and Networks (GLOBECOM GCSN), Technical Program Committee Member.
- IEEE International Conference on Computer Communications and Networks (ICCCN), Technical Program Committee Member.
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), Technical Program Committee.
- IEEE Symposium on Computers and Communications International (ISCC), Technical Program Committee Member.
- ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), Technical Program Committee Member.
- IEEE International Symposium on Quality Electronic Design (ISQED), Technical Program Committee Member.
- IEEE International Symposium on Circuits and Systems (ISCAS), Reviewer Committee Member.
- IEEE International Conference on Omni-layer Intelligent systems (COINS), Circuits and Systems Designs for Artificial Intelligence and the Internet of Things track, Technical Committee Member.

2021:

- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), Technical Program Committee.
- IEEE Symposium on Computers and Communications (ISCC), Technical Program Committee Member.
- ACM/IEEE Design Automation Conference (DAC), AI/ML System Design, Technical Program Committee Member.
- ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), Technical Program Committee Member.
- IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Technical Program Committee Member.

- ACM Great Lakes Symposium on VLSI (GLSVLSI), VLSI Design Track, Technical Program Committee Member.
- IEEE International Symposium on Quality Electronic Design (ISQED), Circuit Design, 3D Integration and Advanced Packaging (ICAP), Technical Program Committee Member.
- IEEE International Symposium on Circuits and Systems (ISCAS), Reviewer Committee Member.

2020:

- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), Technical Program Committee.
- ACM/IEEE Design Automation Conference (DAC), AI/ML System Design, Technical Program Committee.
- IEEE International Symposium on Circuits and Systems (ISCAS), Reviewer Committee Member.
- IEEE International Conference on Electronics Circuits and Systems (ICECS), Technical Program Committee Member.
- IEEE International Symposium on Embedded Mylticore/Many-core Systems-on-Chip (MCSoC), Program Committee Member.
- ACM Great Lakes Symposium on VLSI (GLSVLSI), Program Committee Member.
- IEEE International Symposium on Quality Electronic Design (ISQED), IoT - Design & Smart Sensors, Technical Program Committee Member.

2019:

- IEEE International New Circuits and Systems Conference (NEWCAS), Neural Networks and Neuromorphic Circuits, Reviewer Committee Member.
- IEEE International Conference on Electronics Circuits and Systems (ICECS), Digital Circuits and Embedded Systems, Technical Program Committee Member.
- IEEE International Symposium on Embedded Mylticore/Many-core Systems-on-Chip (MCSoC), Embedded Multicore/Manycore SoC Architectures, Technical Program Committee Member.
- ACM Great Lakes Symposium on VLSI (GLSVLSI), VLSI Design, Technical Program Committee Member.

2018:

- IEEE International Conference on Omni-layer Intelligent systems. (COINS), Internet of Things: From Device, to Edge, and Cloud, Technical Program Committee Member.
- IEEE/ACM International Workshop on Network on Chip Architectures (NoCArc), Technical Program Committee Member.
- IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Digital architectures: NoC, multi- and many-core, hybrid, and reconfigurable, Technical Program Committee Member.
- IEEE International Conference on Electronics Circuits and Systems (ICECS), Digital Circuits and Embedded Systems, Technical Program Committee Member.
- ACM Great Lakes Symposium on VLSI (GLSVLSI), VLSI Design, Technical Program Committee Member.

2017:

- ACM Great Lakes Symposium on VLSI (GLSVLSI), VLSI Systems Track, Technical Program Committee Member.

- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), System Design and Security Track, Technical Program Committee Member.

2016:

- ACM Great Lakes Symposium on VLSI (GLSVLSI), VLSI Systems Track, Technical Program Committee Member.
- IEEE/ACM International Workshop on Network on Chip Architectures (NoCArc), Technical Program Committee Member.

Session Chair in conferences

- IEEE International Symposium on Quality Electronic Design (ISQED), 2022. Session name: Energy Efficiency with Emerging Technologies for the Edge and the Cloud.
- IEEE International Conference on High Performance Switching and Routing (HPSR), 2022. Session name: Approaches and Methods for Monitoring and Management of Edge Computing Systems and Networks.
- ACM/IEEE Design, Automation and Test in Europe Conference (DATE), 2022. Session name: Energy Efficiency with Emerging Technologies for the Edge and the Cloud.
- ACM/IEEE Design Automation Conference (DAC), 2021. Session name: DES4-I Memory - The Workhorse of Machine Learning.
- ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2021. Session name: 3D Stochastic and Approximate Computing.
- IEEE International Conference on Electronics Circuits and Systems (ICECS), 2018. Session name: Memory Management Schemes.

Reviewer activities

- IEEE Transactions on Sustainable Computing
- IEEE Transactions on Computers
- IEEE Transactions on Very Large Scale Integration Systems
- ACM Transactions on Embedded Computing Systems
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE Transactions on Computer Aided Design
- IEEE Embedded System Letters
- ACM/IEEE Design Automation Conference (DAC)
- ACM/IEEE Design Automation and Test in Europe
- IEEE International Symposium on Quality Electronic Design (ISQED)
- ACM Great Lakes Symposium on VLSI (GLSVLSI)
- IEEE International Symposium on Circuits and Systems (ISCAS)
- IEEE International New Circuits and Systems Conference (NEWCAS)
- IEEE International Symposium on Embedded Mylticore/Many-core Systems-on-Chip (MCSoC)
- IEEE International Conference on Very Large Scale Integration (VLSI-SoC)
- IEEE International Conference on Omni-layer Intelligent systems. (COINS)
- IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)

Presentations/Lectures

- *"Advancing the customization and unlocking the poten-tials of future computing systems,"* Research presentation, Department of Computer Science, KIT Karlsruhe, 2021.
- *"Unlocking the potentials of future computing systems: SIU Embedded Systems Software Lab,"* Research presentation, School of Electrical and Computer Engineering, National technical University of Athens, 2020.
- *"Optimizing Performance of GPU Applications with SM Activity Divergence Minimization,"* Paper presentation, ICECS conference, 2018.
- *"DROP: Distributed Run-Time and Power Constraint Mapping for Many-Core Systems,"* Paper presentation, ICECS conference, 2018.
- *"Workload-aware Resource Management Targeting Internet-of-Things,"* Presentation, Huawei IoT Midwest Research Summit, 2018.
- *"Fog Computing and Efficient Resource Management in the era of Internet-of-Video Things (IoVT),"* Paper presentation, ISCAS conference, 2018.
- *"Weather-based road condition estimation in the era of Internet-of-Vehicles (IoV),"* Paper presentation, ISCAS conference, 2018.
- *"A multi-agent based system for run-time distributed resource management,"* Paper presentation, ISCAS conference, 2017.
- *"Performance-aware resource management of multi-threaded applications on many-core systems,"* Paper presentation, GLSVLI conference, 2017.
- *"Distributed Run-time Management for Multi-agent System,"* Project presentation, FORD Motors Company, Dearborn MI, 2016.
- *"Distributed run-time resource management for malleable applications on many-core platforms,"* Paper presentation, DAC conference, 2013.
- *"A Divide and Conquer based Distributed Run-time Mapping Methodology for Many-Core platforms,"* Paper presentation, DATE conference, 2012.
- *"SPARTAN project: Efficient implementation of computer vision algorithms onto reconfigurable platform targeting to space applications,"* Paper presentation, 6^{th} International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), 2011.
- *"Parallel programming and run-time resource management framework for many-core platforms: The 2PARMA approach,"* Paper presentation, 6^{th} International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), 2011.
- *"Mapping Optimisation for Scalable multi-core ARchiTecture: The MOSART approach,"* Paper presentation, IEEE Computer Society Annual Symposium on VLSI (IS-VLSI) 2010.
- *"Systematic Exploration of Energy-Efficient Application-Specific Network-on-Chip Architectures,"* Paper presentation, IEEE Computer Society Annual Symposium on VLSI (IS-VLSI) 2010.
- *"A High-Level Mapping Algorithm Targeting 3D NoC Architectures with Multiple Vdd,"* Paper presentation, IEEE Computer Society Annual Symposium on VLSI (IS-VLSI) 2010.
- *"Microcoded Dynamic Memory allocation for Multi-core Networks-on-Chip,"* Poster presentation, HiPEAC ACACES summer school, 2010.
- *"Temperature-Aware Platfrom Optimizations for 2D and 3D Networks-on-Chip,"* Paper presentation, 4^{o} National Conference of Electrical and Computer Engineering, 2010.
- *"Node Resource Management for DSP Applications on 3D Network-on-Chip architectures,"* Poster presentation , 16^{th} International Conference on Digital Signal Processing (DSP), 2009.

- "*Three Dimensional FPGA Architectures: A Shift Paradigm for Energy-Performance Efficient DSP Implementations,*" Paper presentation, 16^{th} International Conference on Digital Signal Processing (DSP), 2009.

Released software

- **SNN exploration on SpiNNaker neuromorphic hardware**, a tool that extends the SNN conversion toolbox (SNN-TB) and performs efficient exploration of the hardware dependent parameters of the SpiNNaker neuromorphic platform. The goal is to achieve the highest possible accuracy on the SpiNNaker board for a given SNN architecture.
  `https://github.com/embeddedlabsiu/snn_exploration_spinnaker`

- **BACH scheduler**, a bandwidth and cache aware scheduler for Intel based architectures. BACH is part of a run-time system that orchestrates the execution of multi-threaded applications by incorporating user-defined scheduling policies. It operates in user-space on top of Linux-based operating systems.
  `https://github.com/embeddedlabsiu/BACH_scheduler`

- **Adaptive Approximate Computing on CGRAs**, a framework for bridging approximate computing with coarse grain reconfigurable arrays. Each tile hosts a combination of exact and multiple approximate units (multipliers and adders).
  `https://github.com/embeddedlabsiu/adaptive-approximate-computing`

- **DRTRM**, a Distributed Run-Time Resource Management framework for parallel applications on many-core systems. The target platform of DRTRM, is Intel Single Chip Cloud Computer (SCC), although the design is intended for portability. In addition, it can be compiled to simulate execution of a many-core system, using a process per core on a Linux system. DRTM was developed in collaboration with the Microprocessors and Digital Systems Lab from National Technical University of Athens.
  `https://git.microlab.ntua.gr/billtsou/Distributed-Run-Time-Resource-Manager`

Media publicity

- Grant to fund research on solar-powered emergency communications network School of Electrical and Computer Engineering, SIU, Fall 2018 (Link to US news and SIU blog)
- The demo prepared for SIU Open day was one of the most requested activities School of Electrical and Computer Engineering, SIU, Fall 2018 (Link to The Southern Illinoisan)

Languages

Greek	Native	
English	Excellent	*Certificate of Proficiency in English by* University of Michigan
Japanese	Basic Knowledge	*Level 3 Certificate Japanese-Language Proficiency*
French	Basic Knowledge	*DELF A2 Certificate*