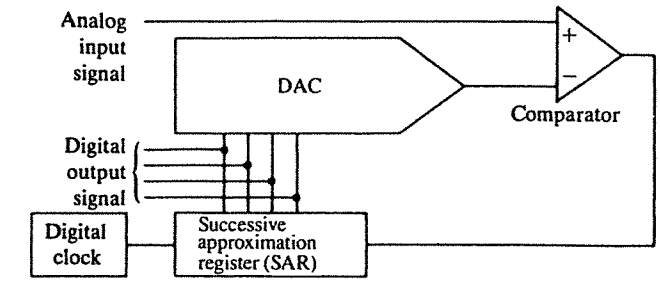
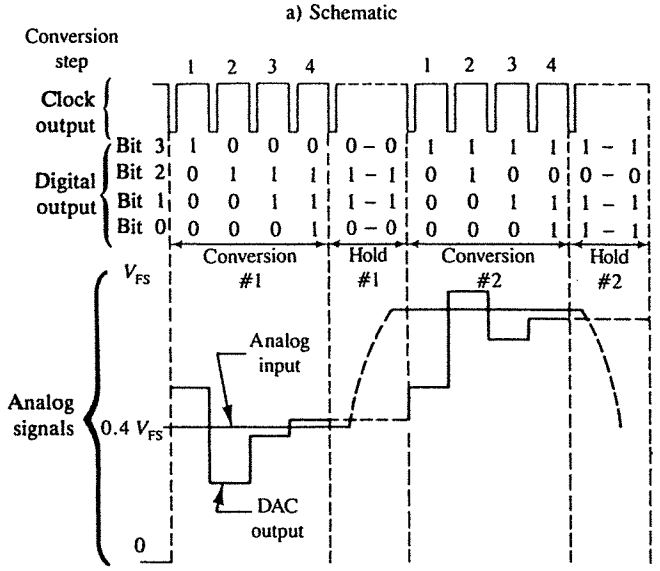


a) Schematic



b) Timing diagram

◆ **Figure 6.36** A 4-bit successive approximation A/D converter. A conversion takes place in four steps, each initiated by a negative clock pulse. The four steps for conversion 1 are as follows:

1. The SAR outputs digital word 1000, producing a DAC output of $V_{FS}/2$ V. This is higher than the analog input, so bit 3 is reset to 0 and latched for the duration of the conversion.
2. The SAR outputs word 0100, producing a DAC output of $V_{FS}/4$ V. This is lower than the analog input, so bit 2 is set to 1 and latched for the duration.
3. The SAR outputs word 0110, producing a DAC output of $3V_{FS}/8$ V. This is lower than the analog input, so bit 1 is set to 1 and latched for the duration.
4. The SAR outputs digital word 0111, producing a DAC output of $7V_{FS}/16$ V. This is higher than the analog input, so bit 0 is reset to 0 and latched for the duration.

The final digital output is 0110.