**EET 438B**

**Sequential Digital Control and Data Acquisition**

**Laboratory 4**

**Analog Measurement and Digital Control Integration Using LabVIEW**

**Laboratory Learning Objectives**

1. Identify the data acquisition card (DAQ) digital input/output voltage and current limitations

2. Identify the electrical characteristics of a TTL digital I/O port used on DAQ cards.

3. Identify the analog voltage input limits of the DAQ system, determine the voltage value of the LSB and the quantization error associated with the analog-to-digital conversion.

4. Determine the input/output characteristic of a non-linear sensor and use logarithms to produce a linear relationship.

4. Design analog scaling circuits using OP AMPs and passive components to minimize the measurement error.

5. Configure analog inputs for both single-ended and differential operation.

6. Develop a LabVIEW program that monitors analog inputs and activates digital control outputs based on a defined sequence of operation.

**Theoretical Background**

DAQ systems have the ability to read and act on both analog and digital inputs. DAQ cards have their digital lines organized into ports comprised of 8 individual lines. Each port line can be configured as an input or an output. These lines are TTL compatible and cannot drive high currents and voltage loads directly.

TTL logic gates are current sinking devices. The inputs of the next gate sources current that the previous device must sink to ground through the chip’s internal circuits. Figure 1 shows the path of current from the input of the sourcing gate to the output of the sinking gate. The TTL specification defines the maximum current an input can source into an output to be 1.6 mA. TTL has a fan-out of 10. This means that up to 10 inputs can connect to a single output line. This means that the maximum current a TTL output can sink is 16 mA.



Figure 1. Current Sinking Path In TTL Gates.

The specifications of each DAQ board give the amount of current that the boards’ digital I/O can sink into various pins. The NI 6221 PCI/PXI board specifications indicate that the digital I/O pins PO0-PO31 can sink 24 mA of current. Digital I/O pins PFI0-PF15 can sink 16 mA. Some computers in the laboratory have the NI-6024E PCI board installed. These devices can sink 24 mA into pin PO0-PO7 and 2.5 mA into pins P10-7, P20-7 and P30-7 respectively.

Figure 2 shows the threshold levels of TTL logic. TTL logic operates on a 5 Vdc supply with an absolute maximum value of 5.25 V. Any voltage level below 0.8 V is a logic "0" while any



Figure 2. Logic Levels for TTL Showing the Threshold Voltage Values

value above 2.4 volts is a logic "1". Voltage levels between 2.0 volts and 0.8 volts are undetermined and usually will not produce a reliable change in gate output. The specified threshold values produces 0.4 V noise immunity for standard TTL signals.

Slowly varying signals on TTL gates can produce unreliable output results. Noisy transitions, such as changing the positions of mechanical switches, also produces spurious outputs. Mechanical switch contacts can make multiple transitions before coming to rest. This mechanical switching transient ends after 20-30 mS typically. Schmitt Trigger TTL gates provide higher levels of noise immunity than regular TTL gates and can turn slowly varying signals into crisp pulses. Interfacing to mechanical switches through Schmitt Trigger gates reduces false triggering due to contact bounce. The act of removing noise and unwanted signals from a digital line is called debouncing. Figure 3 shows a typical digital input line before and after debouncing using a Schmitt Trigger. The 74LS14 TTL device is a hex Schmitt Trigger commonly employed to reduce noise and produce sharp transitions in digital signals.



Figure 3. Noisy Digital Signal Showing Contact and Random Noise.

Current limiting resistors connected to switches restrict the current into a digital port input to acceptable levels. Figure 4 shows a typical configuration. This diagram shows a mechanical switch, connected as a current source that ties the digital input to ground producing a logic low when closed. The resistor is called a "pull-up" resistor, in this case, because is connects the TTL input to the TTL high level. The resistor also restricts the current entering the gate to 2.27 mA, which is slightly more than one unit TTL load. Connecting the series resistor and switch to the gate through a Schmitt Trigger inverter improves noise immunity, debounces the switch and inverts the logic signal producing a logic high when the switch is closed.



Figure 4. Connecting Mechanical Switches to Input Ports: Direct Connect and Through a Schmitt Trigger.

Interfacing to a digital output is best accomplished by sinking current through the port line. This means that the port line output voltage should go to a logic low, connecting the load to ground. Buffer gates or individual transistors provide sufficient current for driving loads that exceed port capabilities. Open collector invertors such as the 74LS06 provide current to loads through an external resistor. Figure 5 shows how this device can sink currents from an external load such as an LED or small electromechanical relay. Higher current loads require external transistors or

.

Figure 5. Digital Interface Using Open Collector TTL Gates.

MOSFETs. Connecting a load to a TTL output using a standard transistor requires a device with sufficient collector current capability to handle the load and the correct sizing of the base resistor. Figure 6 shows the schematic diagram for a BJT interface to a relay. The components



Figure 6. Transistor Interface to an Electromechanical Relay.

Rc and Lc represent the relay coil resistance and inductance respectively. The diode, D1, connects in parallel to the relay coil and suppresses the inductive voltage spike that occurs when switching inductive currents. The value of Vc can be a value greater than the 5 V TTL supply as long as it does not exceed the transistor’s collect-to-emitter voltage, Vce. This circuit requires correct sizing of the transistor base resistor, Rb. Equations (1)-(3) are the design equations for this circuit. The voltage values, Vce,sat and Vbe,sat are the saturation voltage values for the

 (1)

 (2)

 (3)

device collector-to-emitter voltage and base-to-emitter voltage respectively. These are assumed to be Vce,sat=0.4 V and V+=0.8 V for silicon transistors. The parameter hFE is the dc current gain also known as .

Analog input channels have both range and resolution limits base on the hardware implementation. Practical Continuous-to-Discrete converters are called analog-to-digital converters. (ADC’s or A/D’s) These devices take the form of ICs that perform data sampling and conversion to finite length binary values. The act of converting an analog value that has infinite resolution into a finite number of binary values introduces resolution and quantizations errors. Figure 7 shows how an infinite resolution analog sign maps into a 3-bit ADC. The



Figure 7. Resolution and Quantization Errors in ADC Conversion Process.

dashed line indicates the infinite resolution analog input signal line. Note that number of levels represented by the binary patterns is 2n-1, where n is the number of bits in the digital representation. Equation (4) defines the voltage resolution of an ADC in terms of the full scale input (FS) voltage and the number of bits.

 (4)

Where: VLSB= voltage value of the least significant bit

FS = full scale input voltage value

n = number of bits in the conversion.

The quantization error occurs when the actual analog input value does not correspond exactly with the binary mapping. Equation (5) gives the quantization error (Q.E.) in terms of the value of the LSB.

 (5)

There are two types of DAQ boards installed in the lab computers: PCI-6024E and PCI-6221. The PCI-6024E has 16 single-ended, 12 bit analog channels. These channels are software configurable to eight differential input channels.. The maximum guaranteed sampling rate is 200 kS/second (200,000 samples/sec). The 6024E has software selectable bipolar input ranges. Table 1 lists these ranges. All channels are direct coupled (dc coupled) and can measure combined ac and dc voltage levels that do not exceed 11 V with respect to ground.

Table 1. PCI-6024E Analog Input Ranges

|  |  |
| --- | --- |
| **Range** | **Bipolar Voltage Limits** |
| 20 V | ±10 |
| 10 V | ±5 |
| 1 V | ±500 mV |
| 100 mV | ±50 mV |

The PCI-6221 DAQ board also has 16 single-ended, 16 bit analog inputs that are software configurable to 8 differential analog inputs. The maximum sampling rate of this device is 250 kS/second. Table 2 gives the software selectable input voltage ranges for the 6221 DAQ device. Notice that these ranges are different than those of the 6024E. All other specifications are the same as the 6024E.

Table 2. PCI-6221 Analog Input Ranges

|  |  |
| --- | --- |
| **Range** | **Bipolar Voltage Limits** |
| 20 V | ±10 |
| 10 V | ±5 |
| 1 V | ±500 mV |
| 400 mV | ±200 mV |

When interfacing an analog signal, select the input voltage ranges so that the maximum input signal level closely corresponds to the range of the analog input channel. Low level signal should use the 100 and 400 mV ranges given for the two boards.

Notice that both devices have bipolar input values. This allows the input of ac signals but reduces the resolution of the measurement range for dc inputs. For example, a 0-10 Vdc transducer output would easily work with the 20 V range of both boards but this reduces the resolution by a factor of two since the negative half of the range is unused. A scaling circuit similar to those covered in ET 438a provides a way to amplify and shift zero-based dc input signals to preserve measurement resolution.

Figure 8 shows a scaling circuit using two OP AMPs. The OP AMP U1 is a summing amplifier



Figure 8. Scaling Amplifier Circuit Schematic. Transducer Source is Vs1.

that adds the offset voltage Vb to the transducer output Vs1. Setting R3=R2 allows Vb to take the value of b found in the scaling equation. The resistor R3 should be large enough to allow amplification of the Vs1 signal as necessary. The resistors, R4 and R5, of the second OP AMP U2 are set equal to give a stage gain of -1. The resistors R1 and R6 set the amplification factor of the scaling circuit, which corresponds to m in the scaling equation. Equation (6) is the scaling equation, which is just the definition of a linear equation. The variables x and y are analogous to Vo and Vs1 respectively so the equation can be written in terms of the OP AMP resistors and input voltages as Equation (7b). This equation uses R3=R2 to simplify the design. The Zener

 (6)

 (7)

diode D1 and resistor R7 provide a stable voltage source for the value of Vb. Table 3 gives the value of b for the DAQ board ranges in the lab. These are the minimum values of each range. The value of R7 is set to assure that the Zener diode will act as regulator. Typical values are between 470 and 120 ohms. Compute the power dissipation of this resistor and size it for power handling accordingly.

A correct value of Vb in the summing amplifier stage may require R3≠ R2. In that case, set b equal to the second term in 7a, select a resistor value for R3 and a Zener diode voltage level, Vb, and compute the value of R2.

Table 3. Vb Values For Analog Signal Scaling Circuits

|  |  |
| --- | --- |
| **Range** | **b Value (Vdc)** |
| 20 V | -10 |
| 10 V | -5 |
| 1 V | -0.5 |
| 400 mV | -200 mV |
| 100 mV | -50 mV |

Equation (8) relates the value of m to the scalar input and output voltage spans. This is then related to the scaling circuit component values. The resistor R3 was previously selected so the

 (8)

span ratio and R3 determine the sum of R1+R6. Use the next closest standard value for R1 and select a potentiometer value for R6 that allows calibration of the output.

**Scalar Design Example**

A transducer has an output span of 0 to 7.5 Vdc over its useful range. The device must be connected to a PCI-6221 analog channel. Select the correct range and design a scaling circuit based on Figure 8 to achieve maximum resolution of this signal. Determine the value of VLSB and the quantization error.

**Solution**

The span of the device fits into the 10 V range of the 6221 board. We can select any reasonable value (1kΩ< R< 1 MΩ) for R3 and R2. Let R2=R3=100 kΩ. The value of b from Table 3 is -5 V and with resistors R2 and R3 equal b=Vb from (7). We now select values for R4 and R5. Let these be R4=R5=470 kΩ. The ratio of the spans determines the value of m, which then allows us to compute the value of the input resistor string, R6+R1. The equation below shows the span calculation for the given ranges.



The m value allows calculation of the input resistor string. The following equations show the final steps in determining these values.



Divide this value into a standard fix resistor value and a calibrating potentiometer value. R1= 68 kΩ and a R6=10 kΩ potentiometer provide sufficient adjustment range for this circuit. The diode, D1 should be a 5.1 volt Zener diode to provide the 5 V reference required for Vb. The Zener current, IZ, determines the value of resistor R7. Refer to the data sheet of the Zener diode to find this value. The data sheet for the 1N751, 5.1 V device indicates IZ=20 mA. Equation (9) finds the value of R7 for given supply voltages and Zener voltages.

 (9)

Where: Vc = power supply voltage

VZ= Zener regulating voltage

IZ= Zener current

Using the values in this example gives,



Use the next lowest standard value of 470 Ω. Now determine the power rating of the resistor.

The following power formula using the voltage dropped across the resistor computes the resistor power dissipation.



This value indicates that a ¼ Watt resistor is sufficient to handle the power dissipation of the Zener regulator.

Figure 9 shows the completed circuit for this example with all component values included.



Figure 9. Example Circuit Design for Scaling 0-7.5 Vdv to 10 Volt Range.

The number of bit in the ADC and the full scale voltage are required to find the voltage value of the LSB. In this example, VFS=10 V and the number of bits, n=16 for the 6221 device. The value of the VLSB and the quantization error are found from equations (4) and (5)



These values indicate that the smallest discernible voltage value is 153 V, which is well below the electric noise levels of the lab. The quantization error is half the amount of VLSB, which is 76 V. This value is also well below the lab electric noise levels.

**Laboratory Project Overview**

The purpose of this lab is to develop a LED light array controller using a Cadmium-Sulfide photo-resistor as a sensor and four, TTL-compatible SPST relays to control the array’s input current. This requires determination of the sensor input/output characteristic, sensor output voltage scaling, definition of analog and digital I/O using the NI-MAX, and LabVIEW program development. Figure 10 shows an overview of this experiment. A series of resistors controls



Figure 10. Lab 4 Project Overview Showing Major Sub-Systems.

the brightness of the LED array based on a photo-resistor sensor analog input signal. Digital outputs actuate the control relays RC0-RC3 to apply voltage to the array and control the LED currents by shorting out the control resistors R2-R4. Size R1 to allow maximum LED current without damaging the LEDs.

A voltage divider that includes a photo-resistor light sensor turns light level into a voltage. A scaling circuit amplifies this voltage to achieve maximum resolution of the analog input. This signal enters the computer through an analog input channel defined during the project. A LabVIEW program monitors the light level presented in the analog input channel and adjusts the LED brightness by increasing or decreasing the series resistance by opening/closing the control relays.

**Procedure**

1. Determine the photo-resistor light/resistance characteristic. The photo-resistor is a Radioshack Part/Cat. Number 276-1657. Figure 11 shows the test fixture for determining the sensor resistance as for an LED input current. Mechanically



Figure 11. Determining the Relationship Between ILED and Photo-Resistor Resistance

connect the LED to the photo-resistor using a short section of heat-shrink tubing or black electrical tape. Use a T1 sized red LED for the light source. Connect the LED to a 15 Vdc voltage source through a 10 kΩ potentiometer, a current limiting resistor RL and an ammeter as shown in Figure 11. Size RL based on the maximum allowable LED current found in the LED data sheets. Also connect an Ohmmeter to the photo-resistor leads. Vary the LED current starting from 0 to the maximum value in ten steps using the potentiometer. Record ILED and sensor resistances Rs in Table A1. Also note the maximum Rs and ILED in the spaces provided above Table A1.

1. Use Excel to plot the data from Table A1 and save this for the lab report and further use. Plot these data using both linear scales and Log-Log scales. Note the plotted curves in both cases for further use. Use the **Add Trendline** option to find the intercept and slope of the log-log data plot. Display the trend line and the R2 parameter on the graph Take the natural log of both the LED current and Rs before plotting and analyzing the result using **Add Trendline**
2. Select a value of R5 and use Excel to compute the sensor voltage divider output with 15 Vdc input as shown in Figure 10. Plot the results of these calculations. Adjust the value of R5 until the divider’s output range is within the analog input ranges of the DAQ boards installed in the lab and the plot is as linear as possible.
3. View the online videos that show how to create analog and digital I/O points using the N-MAX.
4. Open the NI-MAX software and create four digital output points called RC-0,RC-1, RC-2, RC-3, RC-4. Also create an analog input channel called , “lightsense” without the quotes. Use any analog input point for this channel. The channel should have a differential input and an input range that can accept the voltage range from step 3 above.
5. Evaluate the sensor output and design a scalar circuit that can interface the sensor output to the analog input channel with maximum resolution. Compute the values of all resistors from Figure 8 to produce a scalar circuit that covers a complete DAQ analog input range given the sensor voltage divider output. Document the circuit design with calculations showing resistor value computations and a schematic.
6. Simulate the design using Multisim, Circuitmaker, or LTSpice. Document the results with a circuit printout showing the output values. Use a dc voltage source to simulate the sensor input. Set the dc source to the sensor minimum and maximum values and check the circuit output for correct response.
7. Construct the LED array and size the resistors R1-R4. Compute the value of R1 using the maximum LED current, ILEDmax, from the device datasheet. If a datasheet is not available, use a typical value. Equation (10) gives the formula for finding this value.

 (10)

Where VD is the diodes’ forward voltage drop. This can be measured or found in the device data sheets. The current ILEDmax is the maximum allowable continuous LED current. The factor of three in (10) accounts for the three parallel LED strings in the array. Size the resistors R2-R4 such that the LED current increases in three steps. Table A-2 shows the required current for each step as the relays short the resistors out. The formulas below this table find the resistor values. Calculate the power dissipation of resistors R1-R4 and select resistors such that their power rating is not exceeded. Document the calculations and enter the computed values in Table A-3.

1. Connect the TTL-compatible relays to the digital output channels using connection diagrams from the NI-MAX and the terminal block connection diagram.
2. Connect the light sensor voltage divider to the scaling circuit as shown in Figure 10 and then to the previously defined analog input channel. Use the connection information available in NI-MAX to identify the correct terminals. Make sure the photo-resistor “sees” room light levels.
3. Develop a LabVIEW program that will control the LED array based on the room light levels. Figure 12 shows the desired program interface. A meter display should show the sensor analog voltage. The panel indictor lamps show the condition of the control relays RC0-RC3. A stop button stops program operation. A flow chart in the Appendix gives a possible program structure for achieving the correct functionality required. Write the program and test it with the hardware setup assembled previously.

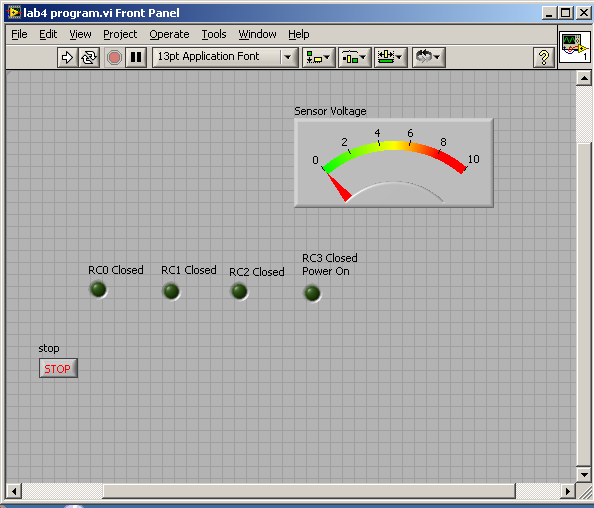


Figure 12. Desired Program Front Panel.

Demonstrate the program to the lab instructor and document it by printing out the front and back panels from the LabVIEW print function.

**Lab 4 Assessments**

Submit the following items for grading and perform the listed actions to complete this laboratory assignment.

1. Submit the photo-resistor log-log plot and lab data generated using Excel. Also submit the raw data taken in the lab and summarized in the Lab 4 Appendix page 15.
2. Submit the scalar design calculations neatly organized on engineering paper.
3. Scalar simulation printout
4. Submit the current limiting resistor calculations (R1-R4). The calculations should include both the resistor values and power dissipation. The calculations should be neatly organized and on engineering paper.
5. The LabVIEW program printout and a 2-5 page double-space program description that explains in detail how the developed program works.
6. Complete the online quiz over the topics covered in this lab. Use all data gathered in the experiment and the lab handout as a reference during the quiz.

**Lab 4 Appendix**

Record ILEDmax here: ILEDmax = \_\_\_\_\_\_\_\_\_\_\_ mA

Record Rs max here: Rs max = \_\_\_\_\_\_\_\_\_\_\_ Ohms (Rs max occurs with ILED=0)

Table A1-Light Sensor Characteristic Data

|  |  |  |
| --- | --- | --- |
| Data  Point | LED Input Current (ILED) mA | Photo-Resistor Rs () |
| 1 |  |  |
| 2 |  |  |
| 3 |  |  |
| 4 |  |  |
| 5 |  |  |
| 6 |  |  |
| 7 |  |  |
| 8 |  |  |
| 9 |  |  |
| 10 |  |  |

Table A-2-LED Current for Each Control Step

|  |  |
| --- | --- |
| Contacts Closed | Desired Current (mA) |
| RC0, RC1, RC2, RC3\* | 3ILEDmax |
| RC0, RC1, RC3 | 2.4ILEDmax |
| RC0, RC3 | 1.5ILEDmax |
| RC3 | ILEDmax |

\*RC3 is the power switch relay and is closed whenever the LEDs’ are energized



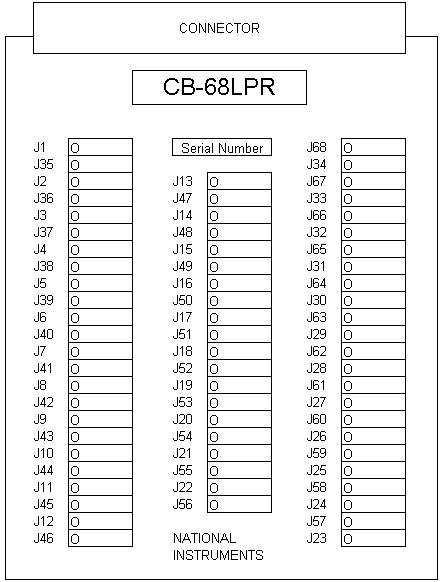
Table A-3-LED Resistor Values and Power Ratings

|  |  |  |  |
| --- | --- | --- | --- |
| Resistor | Value (Ohms) | LED Current (mA) | Power Rating (W) |
| R1 |  |  |  |
| R2 |  |  |  |
| R3 |  |  |  |
| R4 |  |  |  |



Figure A1. LabVIEW Program Flow Chart

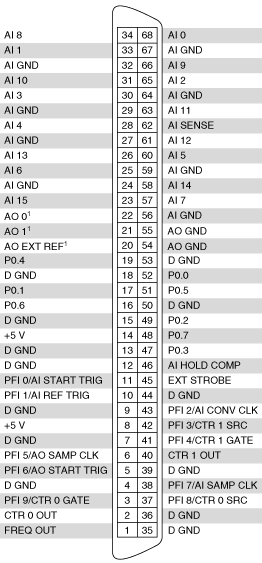
Appendix A –Data Acquisition Interface Pinouts





**68-Pin MIO I/O Connector Pinout**

This figure shows the pinout of 68-pin B Series and E Series devices. If you are using the R6850 or SH6850 cable assemblies with 68-pin E Series devices, refer to the[50-Pin MIO](mk:@MSITStore:C:\Program%20Files\National%20Instruments\NI-DAQ\docs\Device_Pinouts.chm::/50-Pin_MIO_IO_Connector_Pinout.html) pinout.



|  |  |
| --- | --- |
|  | **Note**  Further documentation for the B Series devices is located in the *E Series Help*. |

|  |  |
| --- | --- |
|  | **Note**  Some hardware accessories may not yet reflect the revised terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to the [Terminal Name Equivalents](mk:@MSITStore:C:\Program%20Files\National%20Instruments\NI-DAQ\docs\Device_Pinouts.chm::/Terminal_Name_Equivalents.html) table for information on Traditional NI-DAQ (Legacy) signal names. |

|  |
| --- |
|  |
| 1 No connects appear on pins 20 through 22 of devices that do not support AO or use an external reference.  Old Style Labeling of DAQ board pinouts PCI 6024E |



Shielded Connector Block Pinout

Most Lab DAQ systems use this configuration

