

EET 438B
Sequential Digital Control and Data Acquisition
Laboratory 4
Analog Measurement and Digital Control Integration Using LabVIEW

Laboratory Learning Objectives

1. Identify the data acquisition card (DAQ) digital input/output voltage and current limitations
2. Identify the electrical characteristics of a TTL digital I/O port used on DAQ cards.
3. Identify the analog voltage input limits of the DAQ system, determine the voltage value of the LSB and the quantization error associated with the analog-to-digital conversion.
4. Determine the input/output characteristic of a non-linear sensor and use logarithms to produce a linear relationship.
4. Design analog scaling circuits using OP AMPs and passive components to minimize the measurement error.
5. Configure analog inputs for both single-ended and differential operation.
6. Develop a LabVIEW program that monitors analog inputs and activates digital control outputs based on a defined sequence of operation.

Theoretical Background

DAQ systems have the ability to read and act on both analog and digital inputs. DAQ cards have their digital lines organized into ports comprised of 8 individual lines. Each port line can be configured as an input or an output. These lines are TTL compatible and cannot drive high currents and voltage loads directly.

TTL logic gates are current sinking devices. The inputs of the next gate sources current that the previous device must sink to ground through the chip's internal circuits. Figure 1 shows the path of current from the input of the sourcing gate to the output of the sinking gate. The TTL specification defines the maximum current an input can source into an output to be 1.6 mA. TTL has a fan-out of 10. This means that up to 10 inputs can connect to a single output line. This means that the maximum current a TTL output can sink is 16 mA.

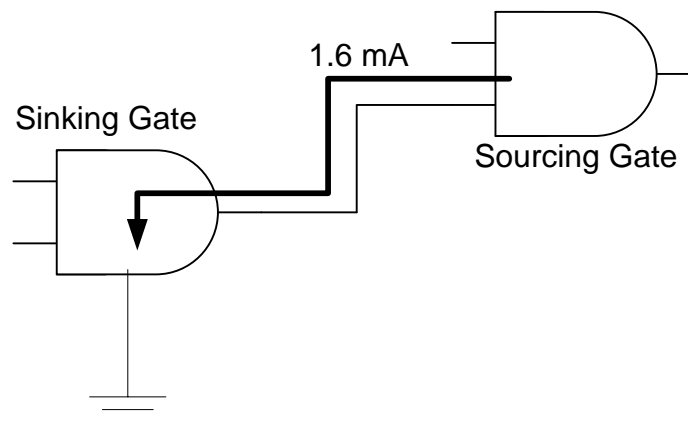


Figure 1. Current Sinking Path In TTL Gates.

The specifications of each DAQ board give the amount of current that the boards' digital I/O can sink into various pins. The NI 6221 PCI/PXI board specifications indicate that the digital I/O pins PO0-PO31 can sink 24 mA of current. Digital I/O pins PFI0-PFI5 can sink 16 mA. Some computers in the laboratory have the NI-6024E PCI board installed. These devices can sink 24 mA into pin PO0-PO7 and 2.5 mA into pins P10-7, P20-7 and P30-7 respectively.

Figure 2 shows the threshold levels of TTL logic. TTL logic operates on a 5 Vdc supply with an absolute maximum value of 5.25 V. Any voltage level below 0.8 V is a logic "0" while any

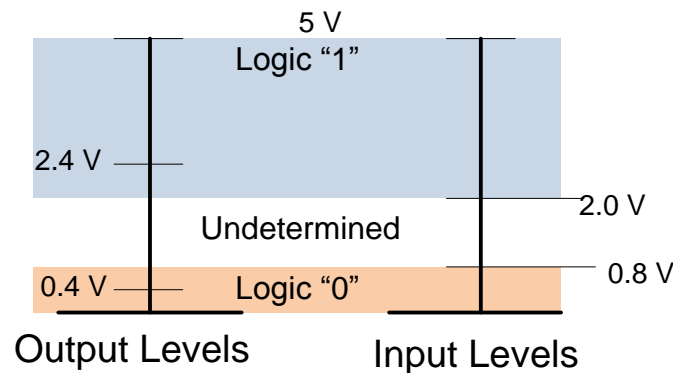


Figure 2. Logic Levels for TTL Showing the Threshold Voltage Values

value above 2.4 volts is a logic "1". Voltage levels between 2.0 volts and 0.8 volts are undetermined and usually will not produce a reliable change in gate output. The specified threshold values produces 0.4 V noise immunity for standard TTL signals.

Slowly varying signals on TTL gates can produce unreliable output results. Noisy transitions, such as changing the positions of mechanical switches, also produces spurious outputs. Mechanical switch contacts can make multiple transitions before coming to rest. This mechanical switching transient ends after 20-30 mS typically. Schmitt Trigger TTL gates provide higher levels of noise immunity than regular TTL gates and can turn slowly varying signals into crisp pulses. Interfacing to mechanical switches through Schmitt Trigger gates reduces false triggering due to contact bounce. The act of removing noise and unwanted signals from a digital line is called debouncing. Figure 3 shows a typical digital input line before and after debouncing using a Schmitt Trigger. The 74LS14 TTL device is a hex Schmitt Trigger commonly employed to reduce noise and produce sharp transitions in digital signals.

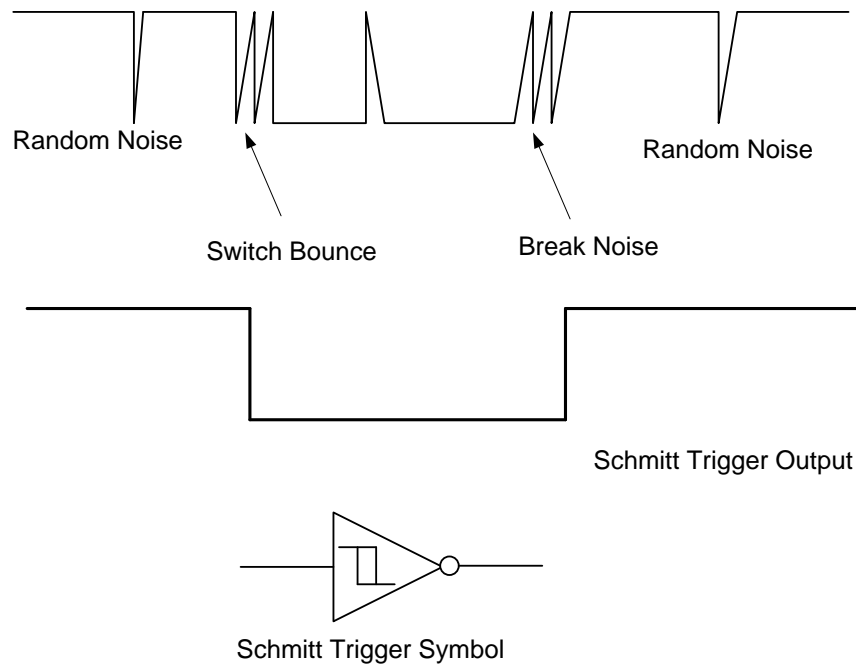


Figure 3. Noisy Digital Signal Showing Contact and Random Noise.

Current limiting resistors connected to switches restrict the current into a digital port input to acceptable levels. Figure 4 shows a typical configuration. This diagram shows a mechanical switch, connected as a current source that ties the digital input to ground producing a logic low when closed. The resistor is called a "pull-up" resistor, in this case, because it connects the TTL input to the TTL high level. The resistor also restricts the current entering the gate to 2.27 mA, which is slightly more than one unit TTL load. Connecting the series resistor and switch to the gate through a Schmitt Trigger inverter improves noise immunity, debounces the switch and inverts the logic signal producing a logic high when the switch is closed.

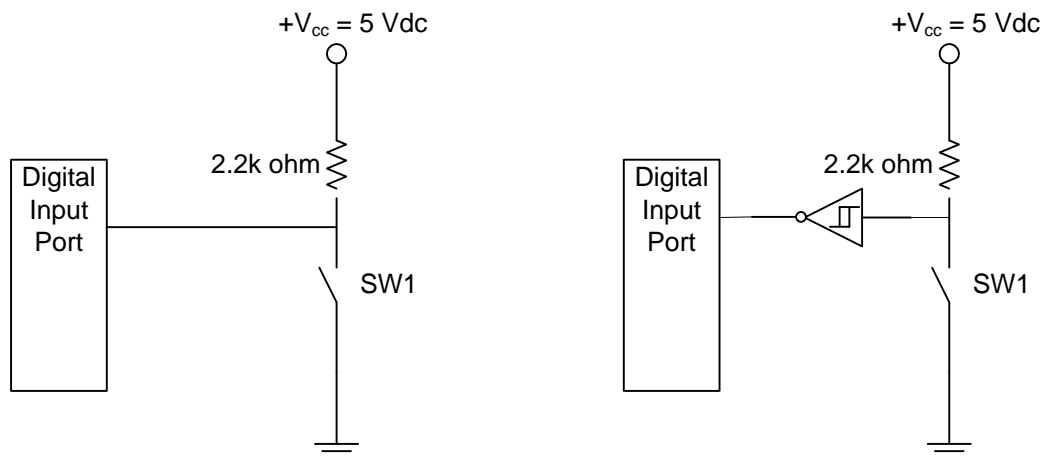


Figure 4. Connecting Mechanical Switches to Input Ports: Direct Connect and Through a Schmitt Trigger.

Interfacing to a digital output is best accomplished by sinking current through the port line. This means that the port line output voltage should go to a logic low, connecting the load to ground.

Buffer gates or individual transistors provide sufficient current for driving loads that exceed port capabilities. Open collector invertors such as the 74LS06 provide current to loads through an external resistor. Figure 5 shows how this device can sink currents from an external load such as an LED or small electromechanical relay. Higher current loads require external transistors or

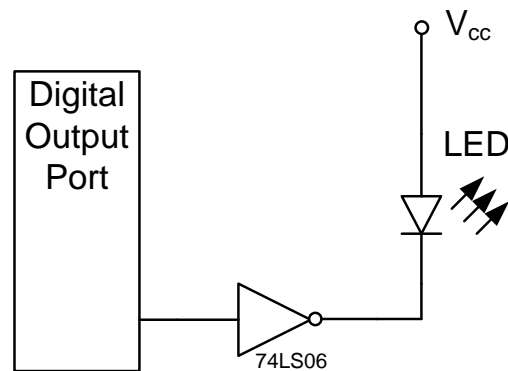


Figure 5. Digital Interface Using Open Collector TTL Gates.

MOSFETs. Connecting a load to a TTL output using a standard transistor requires a device with sufficient collector current capability to handle the load and the correct sizing of the base resistor. Figure 6 shows the schematic diagram for a BJT interface to a relay. The components

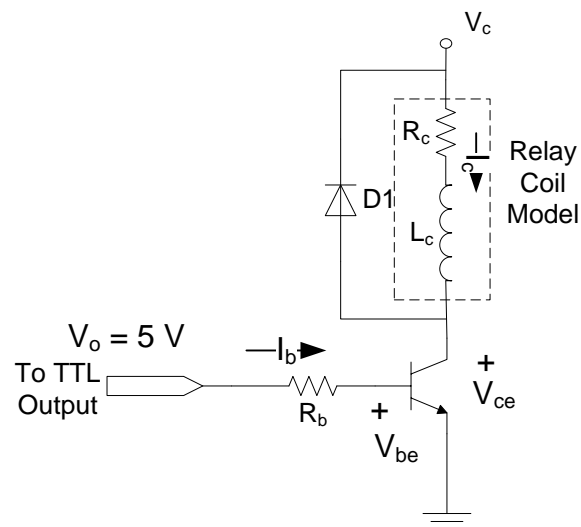


Figure 6. Transistor Interface to an Electromechanical Relay.

R_c and L_c represent the relay coil resistance and inductance respectively. The diode, D1, connects in parallel to the relay coil and suppresses the inductive voltage spike that occurs when switching inductive currents. The value of V_c can be a value greater than the 5 V TTL supply as long as it does not exceed the transistor's collect-to-emitter voltage, V_{ce} . This circuit requires

correct sizing of the transistor base resistor, R_b . Equations (1)-(3) are the design equations for this circuit. The voltage values, $V_{ce,sat}$ and $V_{be,sat}$ are the saturation voltage values for the

$$I_c = \frac{V_c - V_{ce,sat}}{R_c} \quad (1)$$

$$I_b = \frac{I_c}{\left(\frac{h_{FE}}{10}\right)} \quad (2)$$

$$R_b = \frac{V_0 - V_{be,sat}}{I_b} \quad (3)$$

device collector-to-emitter voltage and base-to-emitter voltage respectively. These are assumed to be $V_{ce,sat}=0.4$ V and $V_{be,sat}=0.8$ V for silicon transistors. The parameter h_{FE} is the dc current gain also known as β .

Analog input channels have both range and resolution limits base on the hardware implementation. Practical Continuous-to-Discrete converters are called analog-to-digital converters. (ADC's or A/D's) These devices take the form of ICs that perform data sampling and conversion to finite length binary values. The act of converting an analog value that has infinite resolution into a finite number of binary values introduces resolution and quantizations errors. Figure 7 shows how an infinite resolution analog sign maps into a 3-bit ADC. The

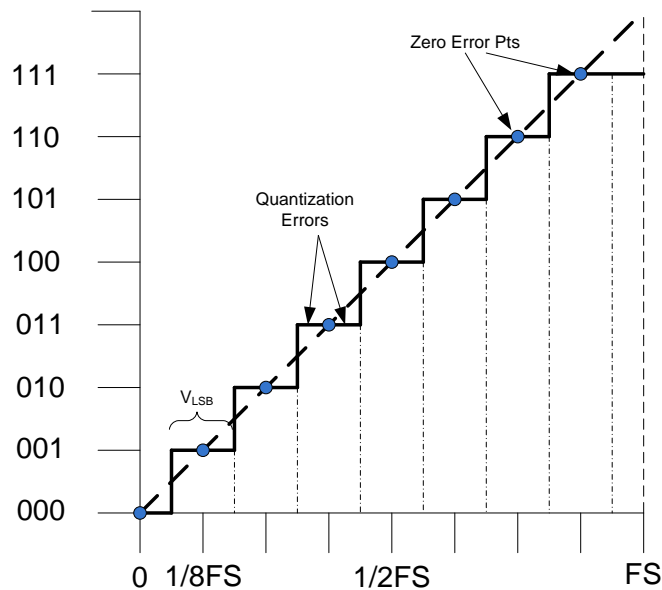


Figure 7. Resolution and Quantization Errors in ADC Conversion Process.

dashed line indicates the infinite resolution analog input signal line. Note that number of levels represented by the binary patterns is $2^n - 1$, where n is the number of bits in the digital representation. Equation (4) defines the voltage resolution of an ADC in terms of the full scale input (FS) voltage and the number of bits.

$$\text{Resolution} = V_{\text{LSB}} = \frac{\text{FS}}{2^n} \quad (4)$$

Where: V_{LSB} = voltage value of the least significant bit
 FS = full scale input voltage value
 n = number of bits in the conversion.

The quantization error occurs when the actual analog input value does not correspond exactly with the binary mapping. Equation (5) gives the quantization error (Q.E.) in terms of the value of the LSB.

$$\text{Q.E.} = \frac{V_{\text{LSB}}}{2} \quad (5)$$

There are two types of DAQ boards installed in the lab computers: PCI-6024E and PCI-6221. The PCI-6024E has 16 single-ended, 12 bit analog channels. These channels are software configurable to eight differential input channels.. The maximum guaranteed sampling rate is 200 kS/second (200,000 samples/sec). The 6024E has software selectable bipolar input ranges. Table 1 lists these ranges. All channels are direct coupled (dc coupled) and can measure combined ac and dc voltage levels that do not exceed 11 V with respect to ground.

Table 1. PCI-6024E Analog Input Ranges

Range	Bipolar Voltage Limits
20 V	± 10
10 V	± 5
1 V	$\pm 500 \text{ mV}$
100 mV	$\pm 50 \text{ mV}$

The PCI-6221 DAQ board also has 16 single-ended, 16 bit analog inputs that are software configurable to 8 differential analog inputs. The maximum sampling rate of this device is 250 kS/second. Table 2 gives the software selectable input voltage ranges for the 6221 DAQ device. Notice that these ranges are different than those of the 6024E. All other specifications are the same as the 6024E.

Table 2. PCI-6221 Analog Input Ranges

Range	Bipolar Voltage Limits
20 V	± 10
10 V	± 5
1 V	$\pm 500 \text{ mV}$
400 mV	$\pm 200 \text{ mV}$

When interfacing an analog signal, select the input voltage ranges so that the maximum input signal level closely corresponds to the range of the analog input channel. Low level signal should use the 100 and 400 mV ranges given for the two boards.

Notice that both devices have bipolar input values. This allows the input of ac signals but reduces the resolution of the measurement range for dc inputs. For example, a 0-10 Vdc transducer output would easily work with the 20 V range of both boards but this reduces the resolution by a factor of two since the negative half of the range is unused. A scaling circuit similar to those covered in ET 438a provides a way to amplify and shift zero-based dc input signals to preserve measurement resolution.

Figure 8 shows a scaling circuit using two OP AMPs. The OP AMP U1 is a summing amplifier

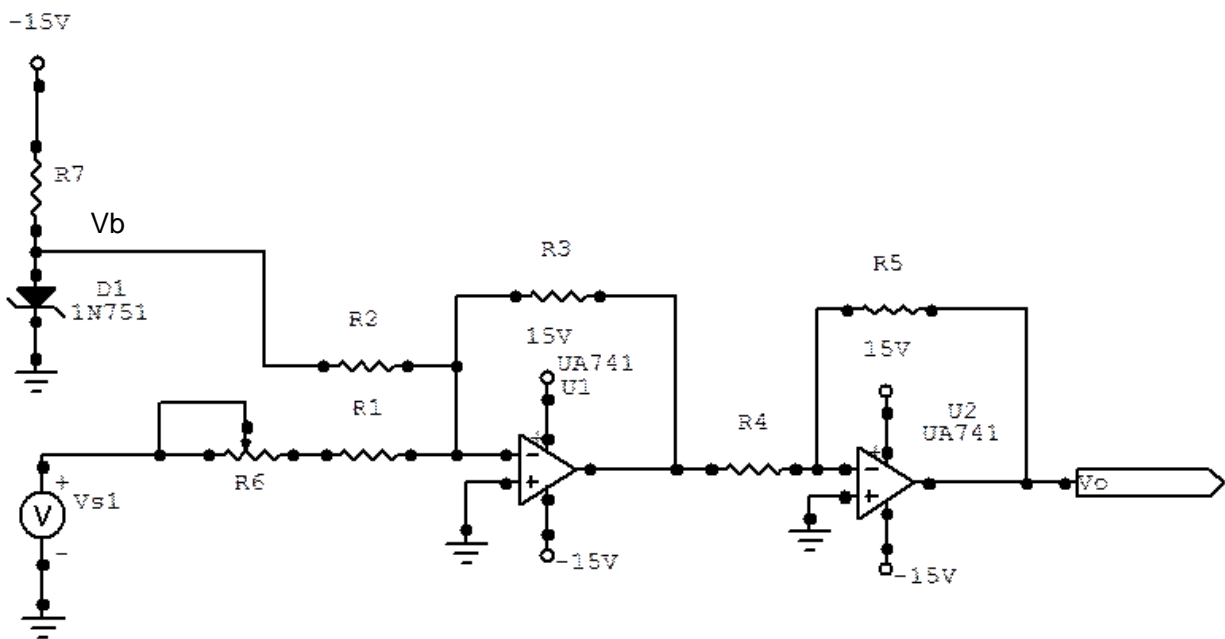


Figure 8. Scaling Amplifier Circuit Schematic. Transducer Source is Vs1.

that adds the offset voltage V_b to the transducer output V_{s1} . Setting $R_3=R_2$ allows V_b to take the value of b found in the scaling equation. The resistor R_3 should be large enough to allow amplification of the V_{s1} signal as necessary. The resistors, R_4 and R_5 , of the second OP AMP U_2 are set equal to give a stage gain of -1. The resistors R_1 and R_6 set the amplification factor of the scaling circuit, which corresponds to m in the scaling equation. Equation (6) is the scaling equation, which is just the definition of a linear equation. The variables x and y are analogous to V_o and V_{s1} respectively so the equation can be written in terms of the OP AMP resistors and input voltages as Equation (7b). This equation uses $R_3=R_2$ to simplify the design. The Zener

$$\begin{aligned}
y &= m \cdot x + b \\
y &\rightarrow V_o \\
x &\rightarrow V_{s1}
\end{aligned} \tag{6}$$

$$\begin{aligned}
V_o &= \left(\frac{R_3}{R_1 + R_6} \right) \cdot V_{s1} + \left(\frac{R_3}{R_2} \right) \cdot V_b \quad (a) \\
R_3 &= R_2 \text{ so} \\
V_o &= \left(\frac{R_3}{R_1 + R_6} \right) \cdot V_{s1} + V_b \quad (b) \\
m &\rightarrow \left(\frac{R_3}{R_1 + R_6} \right) \\
b &\rightarrow V_b
\end{aligned} \tag{7}$$

diode D1 and resistor R7 provide a stable voltage source for the value of V_b . Table 3 gives the value of b for the DAQ board ranges in the lab. These are the minimum values of each range. The value of R7 is set to assure that the Zener diode will act as regulator. Typical values are between 470 and 120 ohms. Compute the power dissipation of this resistor and size it for power handling accordingly.

A correct value of V_b in the summing amplifier stage may require $R_3 \neq R_2$. In that case, set b equal to the second term in 7a, select a resistor value for R_3 and a Zener diode voltage level, V_b , and compute the value of R_2 .

Table 3. V_b Values For Analog Signal Scaling Circuits

Range	b Value (Vdc)
20 V	-10
10 V	-5
1 V	-0.5
400 mV	-200 mV
100 mV	-50 mV

Equation (8) relates the value of m to the scalar input and output voltage spans. This is then related to the scaling circuit component values. The resistor R_3 was previously selected so the

$$m = \frac{V_{o_{\max}} - V_{o_{\min}}}{V_{s1_{\max}} - V_{s1_{\min}}} = \frac{(\text{OutputSpan})}{(\text{InputSpan})} = \left(\frac{R_3}{R_1 + R_6} \right) \tag{8}$$

span ratio and R_3 determine the sum of $R_1 + R_6$. Use the next closest standard value for R_1 and select a potentiometer value for R_6 that allows calibration of the output.

Scalar Design Example

A transducer has an output span of 0 to 7.5 Vdc over its useful range. The device must be connected to a PCI-6221 analog channel. Select the correct range and design a scaling circuit based on Figure 8 to achieve maximum resolution of this signal. Determine the value of V_{LSB} and the quantization error.

Solution

The span of the device fits into the 10 V range of the 6221 board. We can select any reasonable value ($1\text{k}\Omega < R < 1\text{ M}\Omega$) for R_3 and R_2 . Let $R_2=R_3=100\text{ k}\Omega$. The value of b from Table 3 is -5 V and with resistors R_2 and R_3 equal $b=V_b$ from (7). We now select values for R_4 and R_5 . Let these be $R_4=R_5=470\text{ k}\Omega$. The ratio of the spans determines the value of m , which then allows us to compute the value of the input resistor string, R_6+R_1 . The equation below shows the span calculation for the given ranges.

$$m = \frac{V_{o_{\max}} - V_{o_{\min}}}{V_{s1_{\max}} - V_{s1_{\min}}} = \frac{5 - (-5)}{7.5 - 0} = 1.3333$$

The m value allows calculation of the input resistor string. The following equations show the final steps in determining these values.

$$m = \frac{R_3}{R_1 + R_6} = 1.333 = \frac{100\text{ k}\Omega}{R_1 + R_6}$$
$$R_1 + R_6 = \frac{100\text{ k}\Omega}{1.333} = 75\text{ k}\Omega$$

Divide this value into a standard fix resistor value and a calibrating potentiometer value. $R_1 = 68\text{ k}\Omega$ and a $R_6 = 10\text{ k}\Omega$ potentiometer provide sufficient adjustment range for this circuit. The diode, D_1 should be a 5.1 volt Zener diode to provide the 5 V reference required for V_b . The Zener current, I_Z , determines the value of resistor R_7 . Refer to the data sheet of the Zener diode to find this value. The data sheet for the 1N751, 5.1 V device indicates $I_Z = 20\text{ mA}$. Equation (9) finds the value of R_7 for given supply voltages and Zener voltages.

$$R_7 = \frac{V_{cc} - V_Z}{I_Z} \quad (9)$$

Where: V_c = power supply voltage
 V_Z = Zener regulating voltage
 I_Z = Zener current

Using the values in this example gives,

$$R7 = \frac{|-15 - (-5.1)|V}{0.02 A}$$

$$R7 = 495 \Omega$$

Use the next lowest standard value of 470 Ω . Now determine the power rating of the resistor.

The following power formula using the voltage dropped across the resistor computes the resistor power dissipation.

$$P_{R7} = \frac{|-15 - (-5.1)|^2 V}{470 \Omega}$$

$$P_{R7} = 0.209 W$$

This value indicates that a ¼ Watt resistor is sufficient to handle the power dissipation of the Zener regulator.

Figure 9 shows the completed circuit for this example with all component values included.

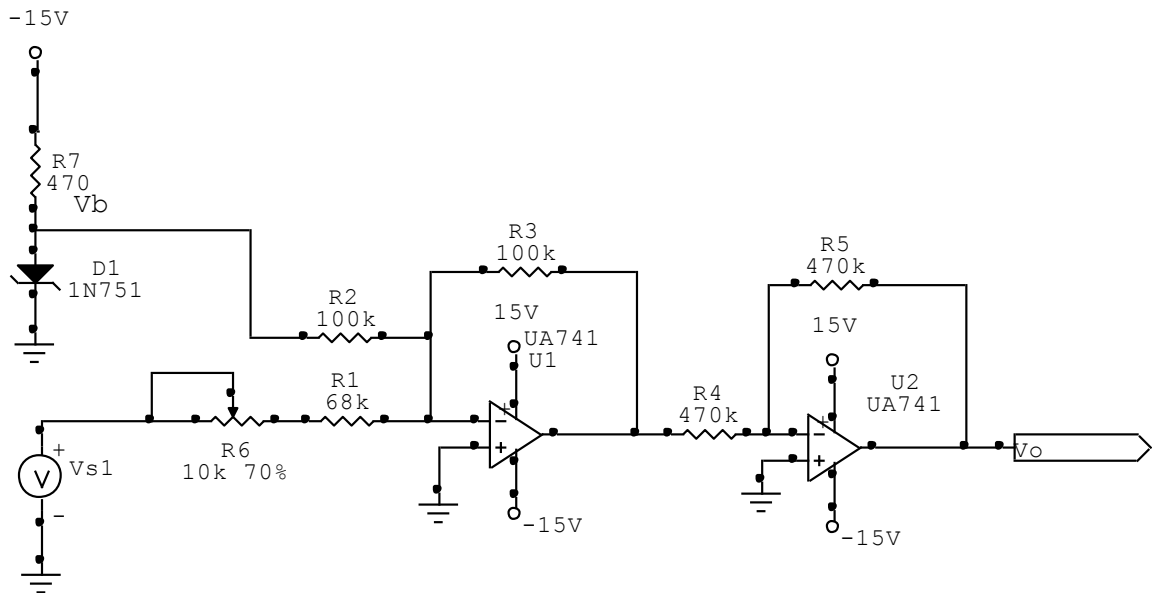


Figure 9. Example Circuit Design for Scaling 0-7.5 Vdv to 10 Volt Range.

The number of bit in the ADC and the full scale voltage are required to find the voltage value of the LSB. In this example, $V_{FS}=10 V$ and the number of bits, $n=16$ for the 6221 device. The value of the V_{LSB} and the quantization error are found from equations (4) and (5)

$$V_{\text{LSB}} = \frac{10}{2^{16}} = 153 \mu\text{V} \quad \text{Q.E.} = \frac{153 \mu\text{V}}{2} = 76 \mu\text{V}$$

These values indicate that the smallest discernible voltage value is 153 μV , which is well below the electric noise levels of the lab. The quantization error is half the amount of V_{LSB} , which is 76 μV . This value is also well below the lab electric noise levels.

Laboratory Project Overview

The purpose of this lab is to develop a LED light array controller using a Cadmium-Sulfide photo-resistor as a sensor and four, TTL-compatible SPST relays to control the array's input current. This requires determination of the sensor input/output characteristic, sensor output voltage scaling, definition of analog and digital I/O using the NI-MAX, and LabVIEW program development. Figure 10 shows an overview of this experiment. A series of resistors controls

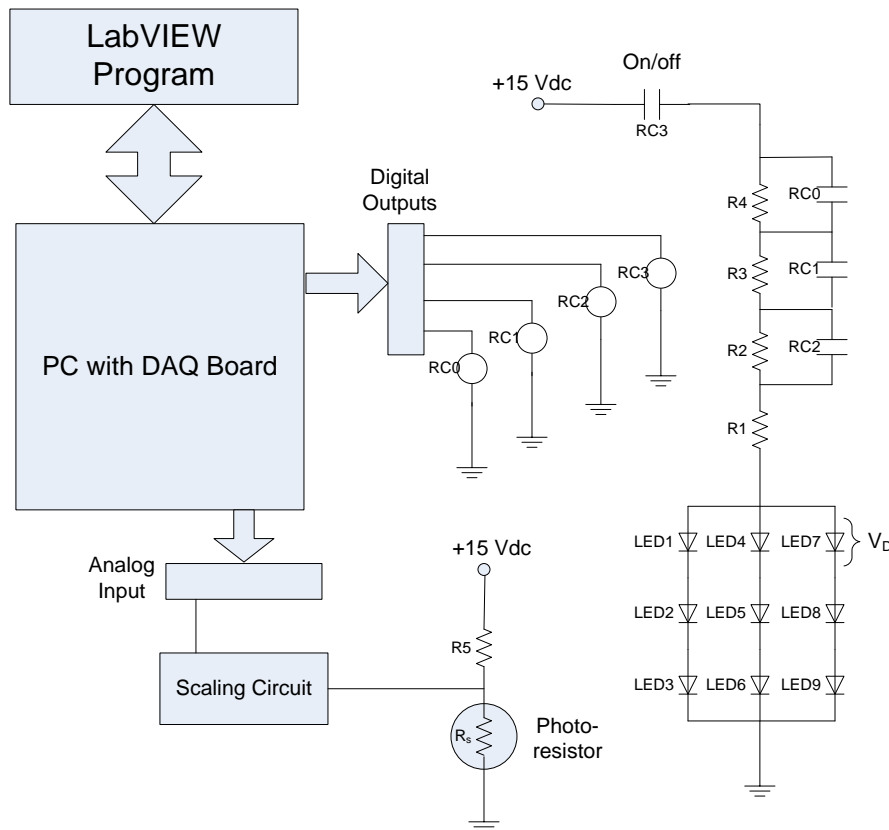


Figure 10. Lab 4 Project Overview Showing Major Sub-Systems.

the brightness of the LED array based on a photo-resistor sensor analog input signal. Digital outputs actuate the control relays RC0-RC3 to apply voltage to the array and control the LED currents by shorting out the control resistors R2-R4. Size R1 to allow maximum LED current without damaging the LEDs.

A voltage divider that includes a photo-resistor light sensor turns light level into a voltage. A scaling circuit amplifies this voltage to achieve maximum resolution of the analog input. This signal enters the computer through an analog input channel defined during the project. A LabVIEW program monitors the light level presented in the analog input channel and adjusts the LED brightness by increasing or decreasing the series resistance by opening/closing the control relays.

Procedure

- 1.) Determine the photo-resistor light/resistance characteristic. The photo-resistor is a Radioshack Part/Cat. Number 276-1657. Figure 11 shows the test fixture for determining the sensor resistance as for an LED input current. Mechanically

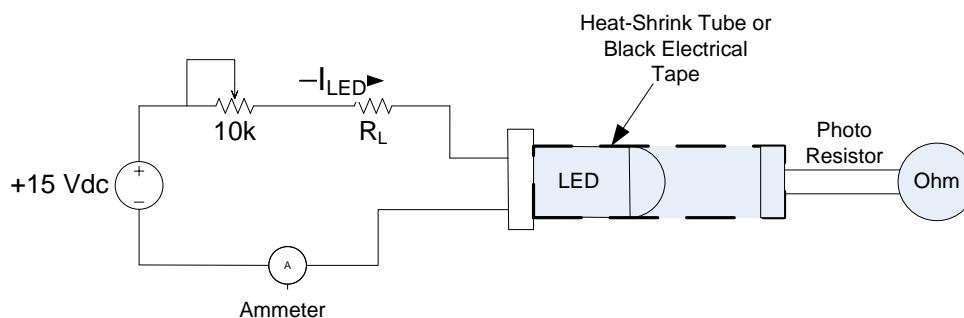


Figure 11. Determining the Relationship Between I_{LED} and Photo-Resistor Resistance

connect the LED to the photo-resistor using a short section of heat-shrink tubing or black electrical tape. Use a T1 sized red LED for the light source. Connect the LED to a 15 Vdc voltage source through a 10 k Ω potentiometer, a current limiting resistor R_L and an ammeter as shown in Figure 11. Size R_L based on the maximum allowable LED current found in the LED data sheets. Also connect an Ohmmeter to the photo-resistor leads. Vary the LED current starting from 0 to the maximum value in ten steps using the potentiometer. Record I_{LED} and sensor resistances R_s in Table A1. Also note the maximum R_s and I_{LED} in the spaces provided above Table A1.

- 2.) Use Excel to plot the data from Table A1 and save this for the lab report and further use. Plot these data using both linear scales and Log-Log scales. Note the plotted curves in both cases for further use. Use the **Add Trendline** option to find the intercept and slope of the log-log data plot. Display the trend line and the R^2 parameter on the graph. Take the natural log of both the LED current and R_s before plotting and analyzing the result using **Add Trendline**.
- 3.) Select a value of R_5 and use Excel to compute the sensor voltage divider output with 15 Vdc input as shown in Figure 10. Plot the results of these calculations. Adjust the value of R_5 until the divider's output range is within the analog input ranges of the DAQ boards installed in the lab and the plot is as linear as possible.

- 4.) View the online videos that show how to create analog and digital I/O points using the NI-MAX.
- 5.) Open the NI-MAX software and create four digital output points called RC-0, RC-1, RC-2, RC-3, RC-4. Also create an analog input channel called , “lightsense” without the quotes. Use any analog input point for this channel. The channel should have a differential input and an input range that can accept the voltage range from step 3 above.
- 6.) Evaluate the sensor output and design a scalar circuit that can interface the sensor output to the analog input channel with maximum resolution. Compute the values of all resistors from Figure 8 to produce a scalar circuit that covers a complete DAQ analog input range given the sensor voltage divider output. Document the circuit design with calculations showing resistor value computations and a schematic.
- 7.) Simulate the design using Multisim, Circuitmaker, or LTSpice. Document the results with a circuit printout showing the output values. Use a dc voltage source to simulate the sensor input. Set the dc source to the sensor minimum and maximum values and check the circuit output for correct response.
- 8.) Construct the LED array and size the resistors R1-R4. Compute the value of R1 using the maximum LED current, I_{LEDmax} from the device datasheet. If a datasheet is not available, use a typical value. Equation (10) gives the formula for finding this value.

$$R1 = \frac{V_c - 3 \cdot V_D}{3 \cdot I_{LEDmax}} \quad (10)$$

Where V_D is the diodes' forward voltage drop. This can be measured or found in the device data sheets. The current I_{LEDmax} is the maximum allowable continuous LED current. The factor of three in (10) accounts for the three parallel LED strings in the array. Size the resistors R2-R4 such that the LED current increases in three steps. Table A-2 shows the required current for each step as the relays short the resistors out. The formulas below this table find the resistor values. Calculate the power dissipation of resistors R1-R4 and select resistors such that their power rating is not exceeded.

Document the calculations and enter the computed values in Table A-3.

- 9.) Connect the TTL-compatible relays to the digital output channels using connection diagrams from the NI-MAX and the terminal block connection diagram.
- 10.) Connect the light sensor voltage divider to the scaling circuit as shown in Figure 10 and then to the previously defined analog input channel. Use the connection information available in NI-MAX to identify the correct terminals. Make sure the photo-resistor “sees” room light levels.
- 11.) Develop a LabVIEW program that will control the LED array based on the room light levels. Figure 12 shows the desired program interface. A meter display should show the sensor analog voltage. The panel indicator lamps show the condition of the control relays RC0-RC3. A stop button stops program operation. A flow chart in the

Appendix gives a possible program structure for achieving the correct functionality required. Write the program and test it with the hardware setup assembled previously.

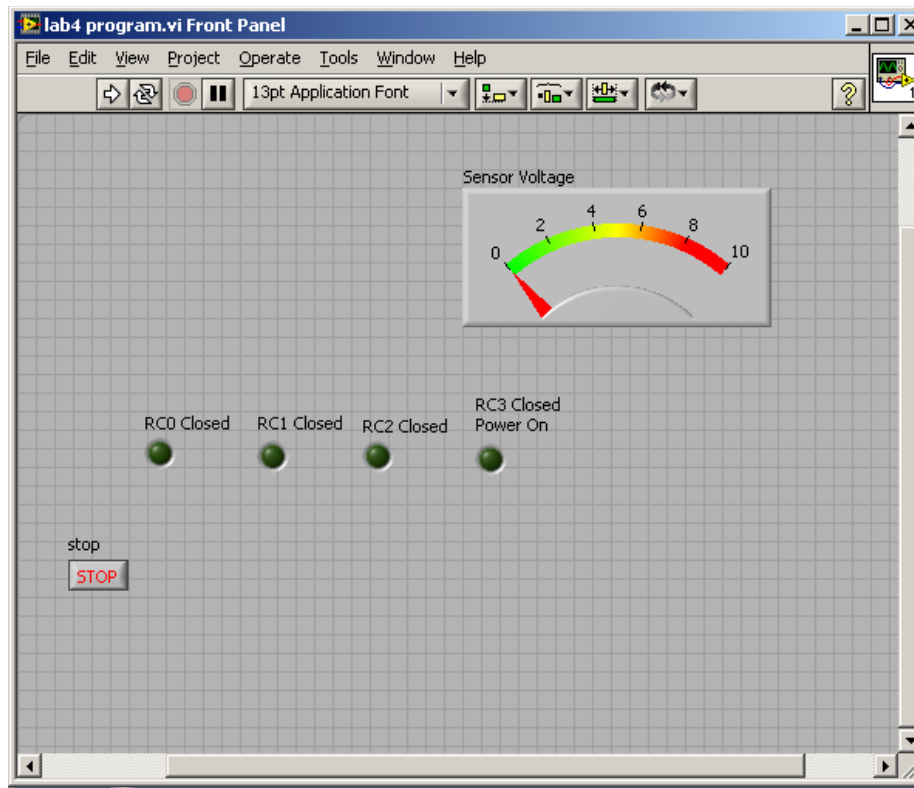


Figure 12. Desired Program Front Panel.

Demonstrate the program to the lab instructor and document it by printing out the front and back panels from the LabVIEW print function.

Lab 4 Assessments

Submit the following items for grading and perform the listed actions to complete this laboratory assignment.

- 1.) Submit the photo-resistor log-log plot and lab data generated using Excel. Also submit the raw data taken in the lab and summarized in the Lab 4 Appendix page 15.
- 2.) Submit the scalar design calculations neatly organized on engineering paper.
- 3.) Scalar simulation printout
- 4.) Submit the current limiting resistor calculations (R1-R4). The calculations should include both the resistor values and power dissipation. The calculations should be neatly organized and on engineering paper.

- 5.) The LabVIEW program printout and a 2-5 page double-space program description that explains in detail how the developed program works.
- 6.) Complete the online quiz over the topics covered in this lab. Use all data gathered in the experiment and the lab handout as a reference during the quiz.

Lab 4 Appendix

Record I_{LEDmax} here: $I_{LEDmax} = \underline{\hspace{2cm}}$ mA

Record R_s max here: $R_s \text{ max} = \underline{\hspace{2cm}}$ Ohms (R_s max occurs with $I_{LED}=0$)

Table A1-Light Sensor Characteristic Data

Data Point	LED Input Current (I_{LED}) mA	Photo-Resistor R_s (Ω)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		

Table A-2-LED Current for Each Control Step

Contacts Closed	Desired Current (mA)
RC0, RC1, RC2, RC3*	$3I_{LEDmax}$
RC0, RC1, RC3	$2.4I_{LEDmax}$
RC0, RC3	$1.5I_{LEDmax}$
RC3	I_{LEDmax}

*RC3 is the power switch relay and is closed whenever the LEDs' are energized

$$R2 = \frac{V_c - 3 \cdot V_D}{2.4 \cdot I_{LED \text{ max}}} - R1$$

$$R3 = \frac{V_c - 3 \cdot V_D}{1.5 \cdot I_{LED \text{ max}}} - (R1 + R2)$$

$$R4 = \frac{V_c - 3 \cdot V_D}{I_{LED \text{ max}}} - (R1 + R2 + R3)$$

Table A-3-LED Resistor Values and Power Ratings

Resistor	Value (Ohms)	LED Current (mA)	Power Rating (W)
R1			
R2			
R3			
R4			

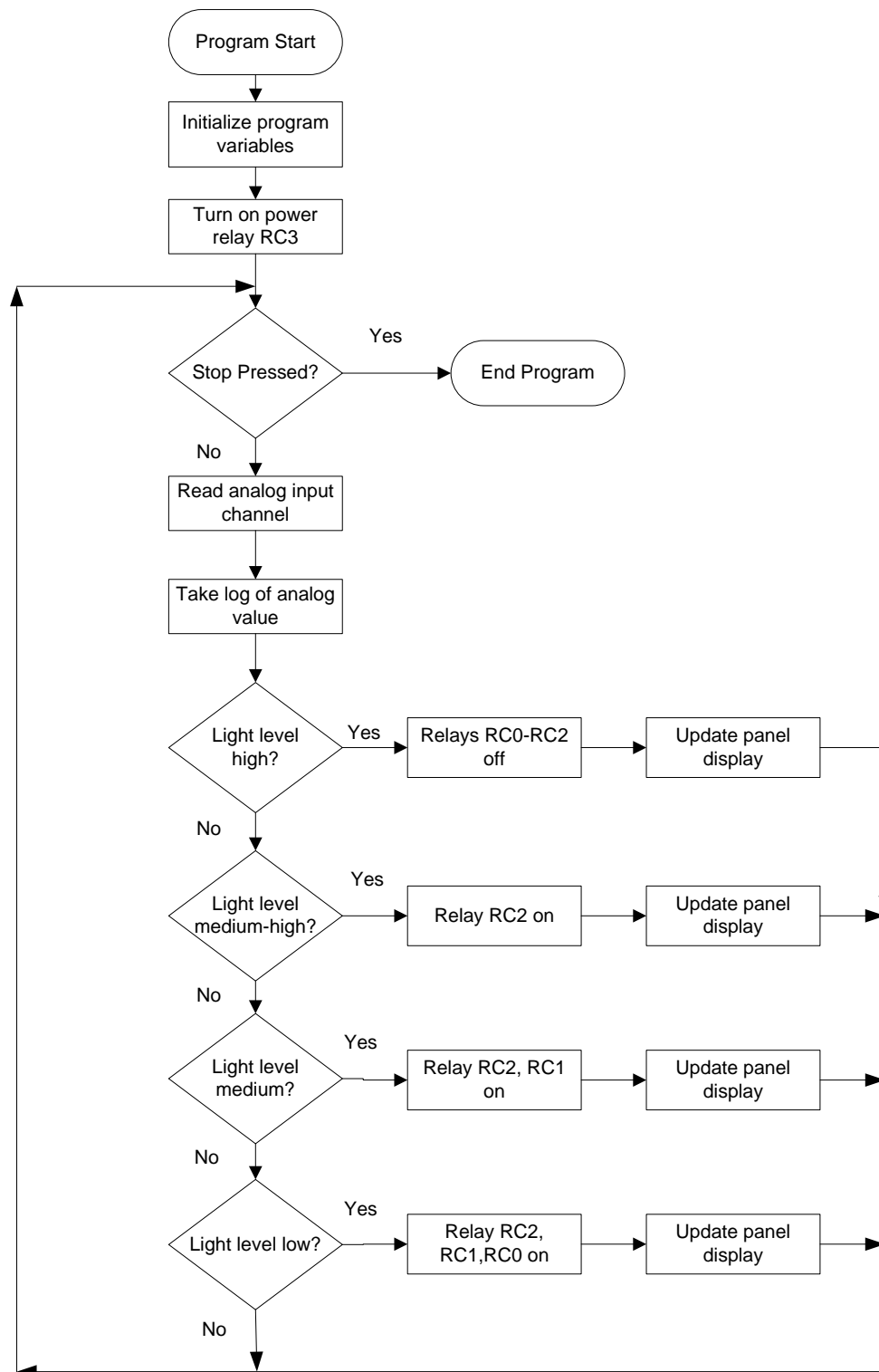
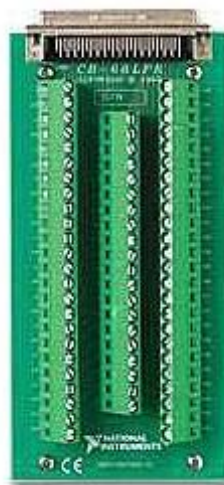
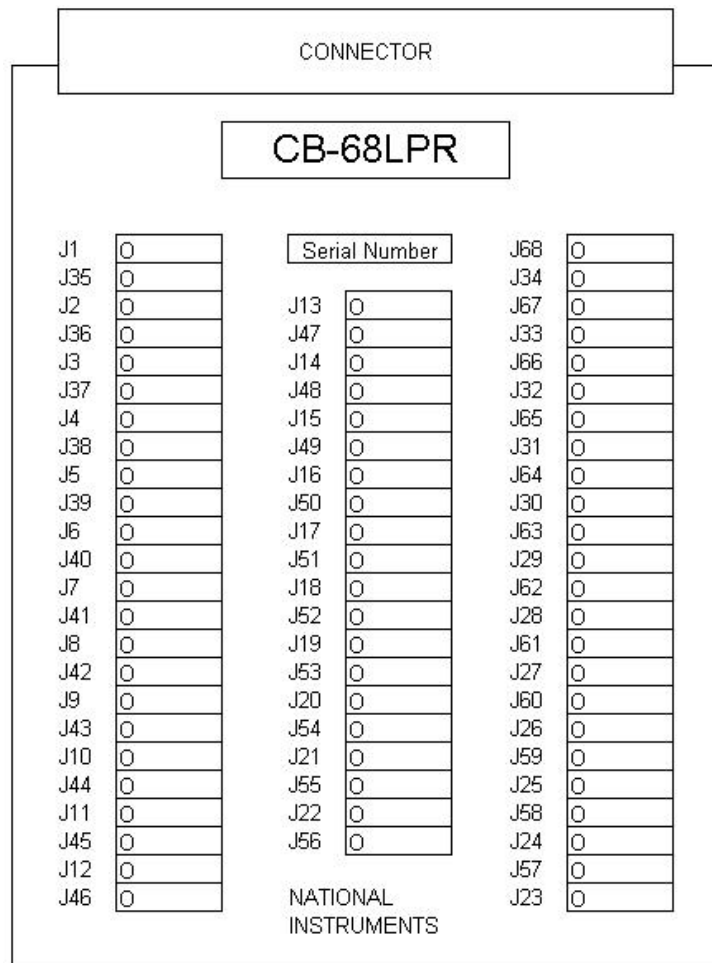


Figure A1. LabVIEW Program Flow Chart

Appendix A –Data Acquisition Interface Pinouts



68-Pin MIO I/O Connector Pinout

This figure shows the pinout of 68-pin B Series and E Series devices. If you are using the R6850 or SH6850 cable assemblies with 68-pin E Series devices, refer to the [50-Pin MIO](#) pinout.

AI 8	34	68	AI 0
AI 1	33	67	AI GND
AI GND	32	66	AI 9
AI 10	31	65	AI 2
AI 3	30	64	AI GND
AI GND	29	63	AI 11
AI 4	28	62	AI SENSE
AI GND	27	61	AI 12
AI 13	26	60	AI 5
AI 6	25	59	AI GND
AI GND	24	58	AI 14
AI 15	23	57	AI 7
AO 0 ¹	22	56	AI GND
AO 1 ¹	21	55	AO GND
AO EXT REF ¹	20	54	AO GND
P0.4	19	53	D GND
D GND	18	52	P0.0
P0.1	17	51	P0.5
P0.6	16	50	D GND
D GND	15	49	P0.2
+5 V	14	48	P0.7
D GND	13	47	P0.3
D GND	12	46	AI HOLD COMP
PFI 0/AI START TRIG	11	45	EXT STROBE
PFI 1/AI REF TRIG	10	44	D GND
D GND	9	43	PFI 2/AI CONV CLK
+5 V	8	42	PFI 3/CTR 1 SRC
D GND	7	41	PFI 4/CTR 1 GATE
PFI 5/AO SAMP CLK	6	40	CTR 1 OUT
PFI 6/AO START TRIG	5	39	D GND
D GND	4	38	PFI 7/AI SAMP CLK
PFI 9/CTR 0 GATE	3	37	PFI 8/CTR 0 SRC
CTR 0 OUT	2	36	D GND
FREQ OUT	1	35	D GND

Note Further documentation for the B Series devices is located in the *E Series Help*.

Note Some hardware accessories may not yet reflect the revised terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to the [Terminal Name Equivalents](#) table for information on Traditional NI-DAQ (Legacy) signal names.

¹ No connects appear on pins 20 through 22 of devices that do not support AO or use an external reference.

Old Style Labeling of DAQ board pinouts PCI 6024E

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT ¹	22	56	AIGND
DAC1OUT ¹	21	55	AOGND ¹
EXTREF ¹	20	54	AOGND ¹
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI8/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

¹ Not available on AT-AI-16XE-10, PCI-6032E, DAQCard-AI-16E-4, DAQCard-AI-16XE-50

Figure 3. 68-Pin I/O Connector for NI 6070E, NI 6060E, NI 6062E, NI 6052E, NI 6041E, NI 6040E, NI 6036E, NI 6035E, NI 6034E, NI 6032E, NI 6030E, NI 6024E, NI 6023E, NI 6020E, NI 6012E and NI 6011E Devices

Shielded Connector Block Pinout
Most Lab DAQ systems use this configuration

SCB-68 Quick Reference Label

E SERIES DEVICES

P/N 182509B-01

FACTORY DEFAULT SETTING

* TEMP. SENSOR DISABLED
* ACCESSORY POWER ON

* TEMP. SENSOR ENABLED
ON SINGLE ENDED CH. 0
* ACCESSORY POWER ON

* TEMP. SENSOR ENABLED
ON DIFFERENTIAL CH. 0
* ACCESSORY POWER ON

* 68 GENERIC TERMINALS
(TEMP. SENSOR AND
ACCESSORY POWER OFF)

PIN # SIGNAL

68	ACH0
34	ACH8
67	AIGND
33	ACH1
66	ACH9
32	AIGND
65	ACH2
31	ACH10
64	AIGND
30	ACH3
63	ACH11
29	AIGND
62	AISENSE
28	ACH4
61	ACH12
27	AIGND
60	ACH5
26	ACH13
59	AIGND
25	ACH6
58	ACH14
24	AIGND
57	ACH7
23	ACH15

PIN # SIGNAL

12	DGND
46	SCANCLK
13	DGND
47	DIO3
14	+5V
48	DIO7
15	DGND
49	DIO2
16	DIO6
50	DGND
17	DIO1
51	DIO5
18	DGND
52	DIO0
19	DIO4
53	DGND
20	EXTREF
54	AOGND
21	DAC1 OUT
55	AOGND
22	DAC0 OUT
56	AIGND

PIN # SIGNAL

1	FREQ_OUT
35	DGND
2	GPCTR0_OUT
36	DGND
3	PFI9/GPCTR0_GATE
37	PFI8/GPCTR0_SOURCE
4	DGND
38	PFI7/STARTSCAN
5	PFI6/WFTRIG
39	DGND
6	PFI5/UPDATE*
40	GPCTR1_OUT
7	DGND
41	PFI4/GPCTR1_GATE
8	+5V, FUSED
42	PFI3/GPCTR1_SOURCE
9	DGND
43	PFI2/CONVERT*
10	PFI1/TRIG2
44	DGND
11	PFI0/TRIG1
45	EXTSTROBE*

Figure B-1. E Series Devices